

# SPPU-SE-COMP-CONTENT - KSKA Git

## Assignment No. 4

Title: Comparator

Problem Statement: Verify the truth table of one bit and two bit comparators using logic gates and comparator IC.

Hardware and

Software

Requirements

Theory:

1) What is comparator?

- A digital comparator or magnitude comparator is a hardware electronic device that takes two numbers as input in binary form and determines whether one number is greater than, less than or equal to the other number.

- Comparators are used in Central Processing Units (CPUs) and microcontrollers (MCUs).

2) IC-7485 Description

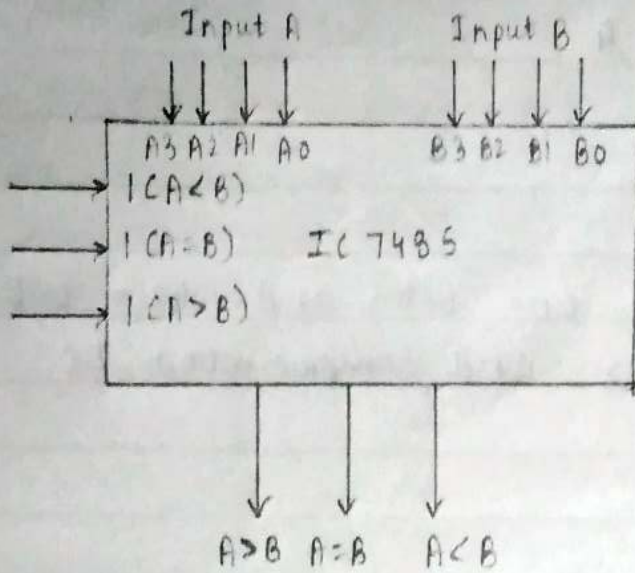
- ~~9-bit~~ It is an 8-bit magnitude comparator.

- It compares

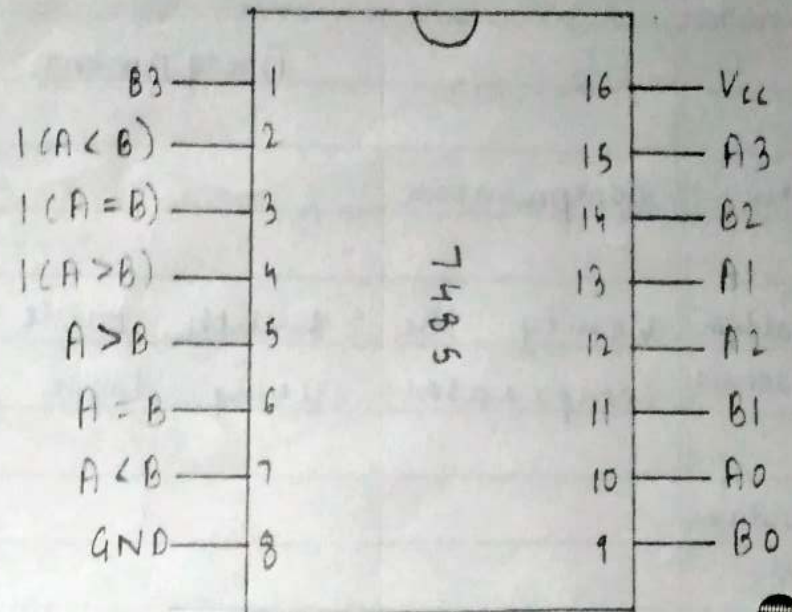
i) 4-bit Magnitude Comparator

- The 4-bit comparator is mostly available in IC form and common type of this IC is 7485. This IC can be used to compare two 4-bit binary words by grounding  $I(A > B)$ ,  $I(A < B)$ ,  $I(A = B)$  connectors

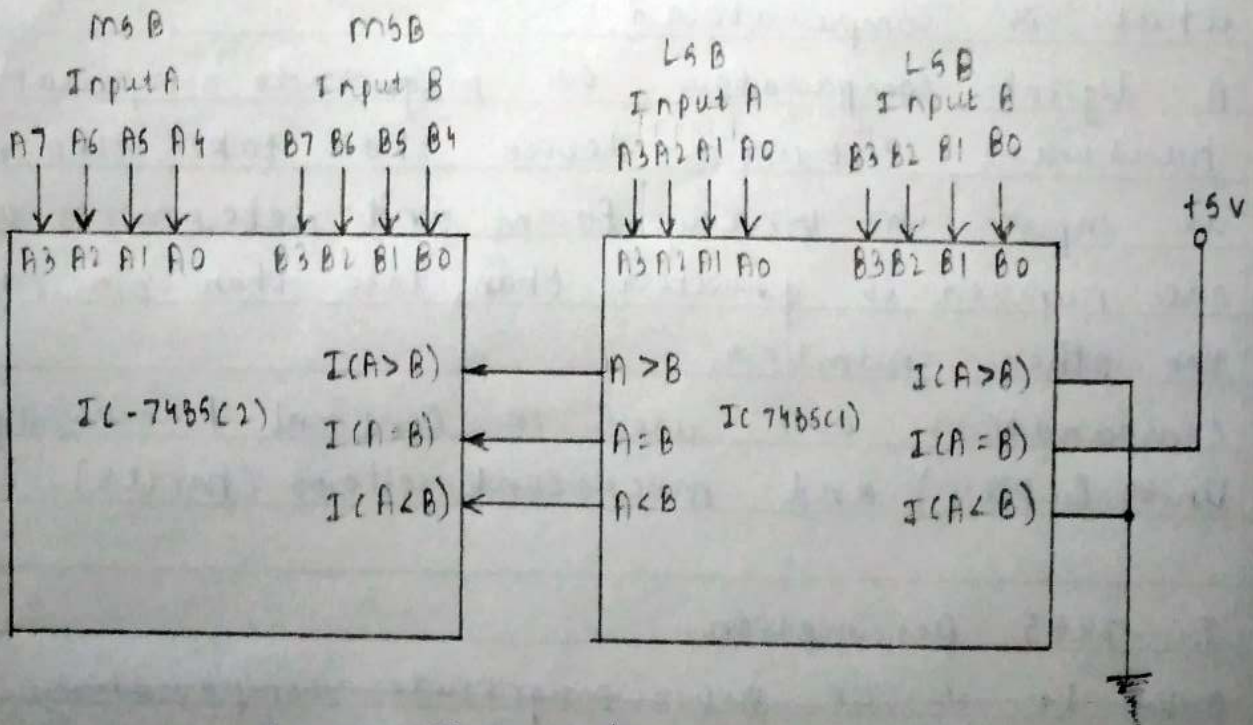
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4-bit Magnitude Comparator



pin description



8-bit Magnitude Comparator

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inputs to  $V_{cc}$  terminal.

## (ii) 8-bit Magnitude Comparator

- An 8-bit comparator compares the two 8-bit numbers by cascading of two 4-bit comparators.
- The circuit connection of this comparator is shown below in which the lower order comparator  $A < B$ ,  $A = B$  and  $A > B$  outputs are connected to the respective cascade inputs of the higher order comparator.

## Design:

- 1-bit comparator
- Truth table

A	B	$A > B$	$A = B$	$A < B$
0	0	0	1	0
0	1	0	0	1
1	0	1	0	0
1	1	0	1	0

## • K-map:

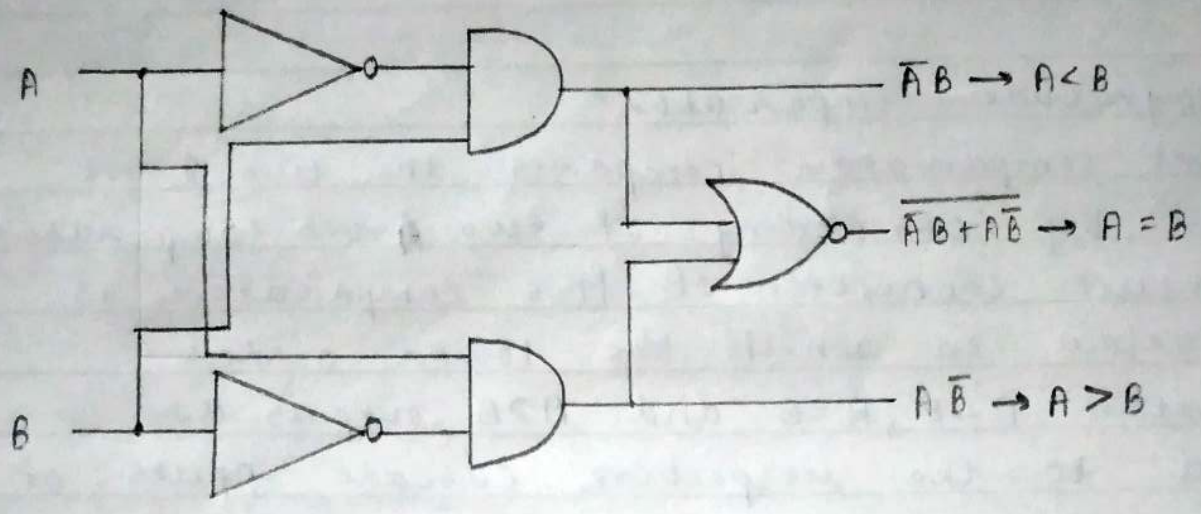
(i)  $A > B$

	$A > B$	
	B	$\bar{B}$
$\bar{A}$	0	0
A	1	0

$$\therefore A > B = A\bar{B}$$

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→ Circuit diagram:



A	B	A < B	A = B	A > B
0	0	0	1	0
0	1	0	0	1
1	0	1	0	0
1	1	0	1	0

ii)  $A = B$

		$A = B$	
		$B$	$\bar{B}$
$A$	$\bar{A}$	1	0
	$A$	0	1
		2	3

$$(A = B) = \bar{A}\bar{B} + AB$$

$$= \overline{AB + \bar{A}\bar{B}}$$

iii)  $A < B$

		$A < B$	
		$B$	$\bar{B}$
$A$	$\bar{A}$	0	1
	$A$	0	0
		2	3

$$A < B = \bar{A}B$$

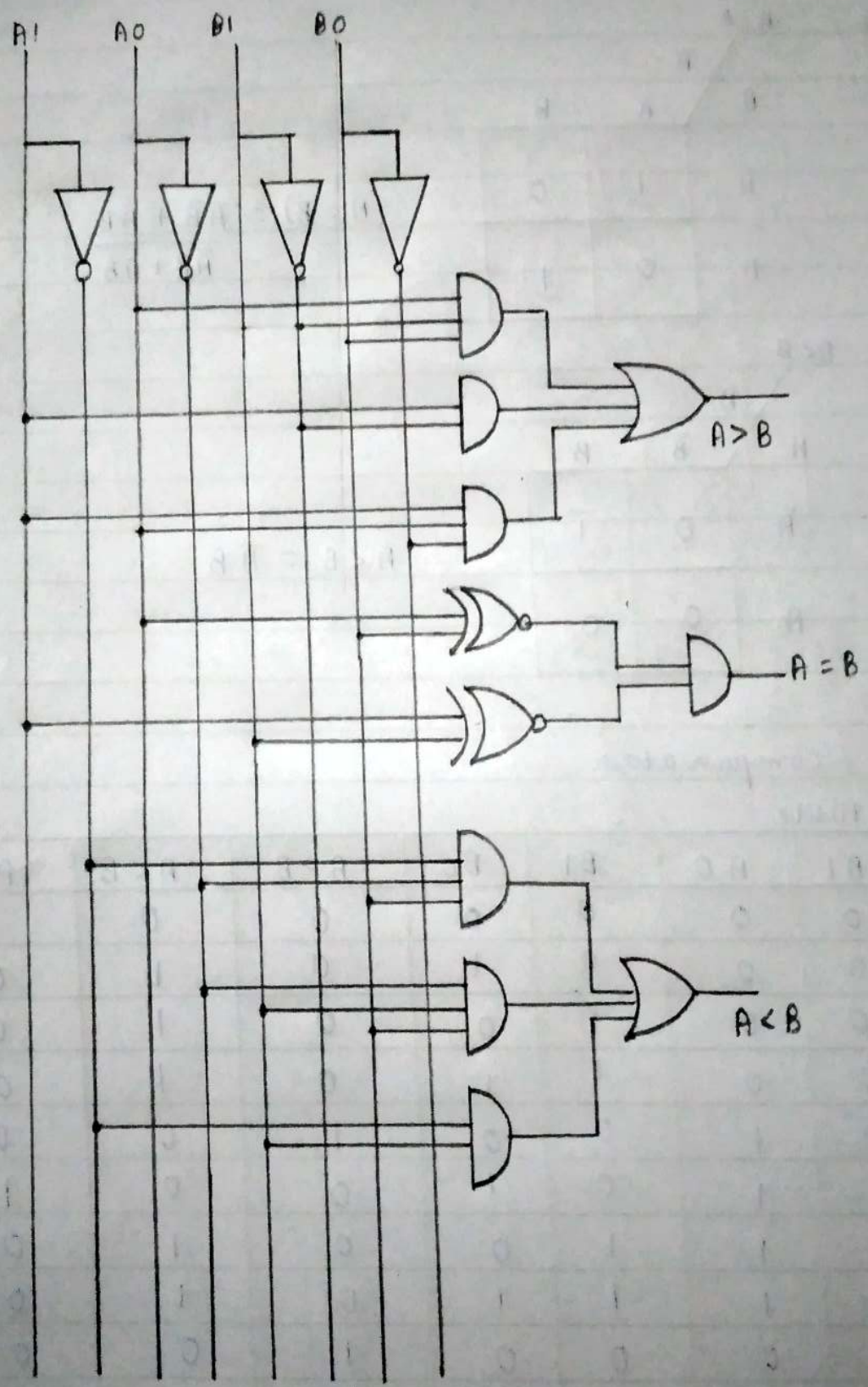
2. 2-bit Comparator

• Truth Table

	A1	A0	B1	B0	A > B	A < B	A = B
	0	0	0	0	0	0	1
	0	0	0	1	0	1	0
	0	0	1	0	0	1	0
	0	0	1	1	0	1	0
	0	1	0	0	1	0	0
	0	1	0	1	0	0	1
	0	1	1	0	0	1	0
	0	1	1	1	0	1	0
	1	0	0	0	1	0	0
	1	0	0	1	1	0	0
	1	0	1	0	0	0	1
	1	0	1	1	0	1	0
	1	1	0	0	1	0	0
	1	1	0	1	1	0	0
	1	1	1	0	1	0	0
	1	1	1	1	0	0	1

→ Circuit diagram:-

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• K-map A > B

i) A > B

		B I B O			
A I A O		$\bar{B} \bar{B} O$	$\bar{B} B O$	$B \bar{B} O$	$B B O$
$\bar{A} \bar{A} O$		0 <sub>0</sub>	0 <sub>1</sub>	0 <sub>3</sub>	0 <sub>2</sub>
$\bar{A} A O$		1 <sub>4</sub>	0 <sub>5</sub>	0 <sub>7</sub>	0 <sub>6</sub>
A I A O		1 <sub>12</sub>	1 <sub>13</sub>	0 <sub>15</sub>	1 <sub>14</sub>
A I $\bar{A} O$		1 <sub>8</sub>	1 <sub>9</sub>	0 <sub>11</sub>	0 <sub>10</sub>

$$A > B = A \bar{B} \bar{B} + A O \bar{B} \bar{B} O + A I A O \bar{B} O$$

ii) A = B

		B I B O			
A I A O		$\bar{B} \bar{B} O$	$\bar{B} B O$	$B \bar{B} O$	$B B O$
$\bar{A} \bar{A} O$		1 <sub>0</sub>	0 <sub>1</sub>	0 <sub>3</sub>	0 <sub>2</sub>
$\bar{A} A O$		0 <sub>4</sub>	1 <sub>5</sub>	0 <sub>7</sub>	0 <sub>6</sub>
A I A O		0 <sub>12</sub>	0 <sub>13</sub>	1 <sub>15</sub>	0 <sub>14</sub>
A I $\bar{A} O$		0 <sub>8</sub>	0 <sub>9</sub>	0 <sub>11</sub>	1 <sub>10</sub>

$$\begin{aligned} (A=B) &= \bar{A} \bar{A} O \bar{B} \bar{B} O + \bar{A} I A O \bar{B} B O + A I A O B \bar{B} O + A I \bar{A} O B B O \\ &= \bar{A} O \bar{B} O (\bar{A} \bar{B} \bar{B} + A B B) + A O B O (\bar{A} \bar{B} \bar{B} + A B B) \\ &= (\bar{A} \bar{B} \bar{B} + A B B) (\bar{A} O \bar{B} O + A O B O) \\ &= (\bar{A} \odot \bar{B}) (\bar{A} \odot \bar{B}) \end{aligned}$$

iii) A < B

		B I B O			
A I A O		$\bar{B} \bar{B} O$	$\bar{B} B O$	$B \bar{B} O$	$B B O$
$\bar{A} \bar{A} O$		0 <sub>0</sub>	1 <sub>1</sub>	1 <sub>3</sub>	1 <sub>2</sub>
$\bar{A} A O$		0 <sub>4</sub>	0 <sub>5</sub>	1 <sub>7</sub>	1 <sub>6</sub>
A I A O		0 <sub>12</sub>	0 <sub>13</sub>	0 <sub>15</sub>	0 <sub>14</sub>
A I $\bar{A} O$		0 <sub>8</sub>	0 <sub>9</sub>	1 <sub>11</sub>	0 <sub>10</sub>

$$A < B = \bar{A} \bar{B} \bar{B} + \bar{A} \bar{A} O \bar{B} O + \bar{A} O B B O$$

Conclusion: Verified the result table of one bit and two bit comparators using logic gates and comparator IC.

A	B	Y <sub>1</sub>	Y <sub>2</sub>	Y <sub>3</sub>
0	0	0	0	0
0	1	0	1	0
1	0	1	0	0
1	1	0	0	1

A	B	Y <sub>1</sub>	Y <sub>2</sub>	Y <sub>3</sub>
0	0	0	0	0
0	1	0	1	0
1	0	1	0	0
1	1	0	0	1