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Assignment 5

Title: Parity Generator

Problem Statement: Design and Implement Parity Generator using EX-OR

Hardware and Software Requirements

Theory:

1) What is Parity ?

- A term used to specify the number of ones in a digital word.
- There are two types of parity :- even and odd.
- An even parity generator will produce a logic 1 at its output if the data word contains an odd number of ones.
- An odd parity generator will produce a logic 1 at its output if the data word contains an even number of ones.

3) Even / Odd Parity Example

7 bits of data	count of 1-bits	8-bits including parity	
		even	odd
0000000	0	00000000	10000000

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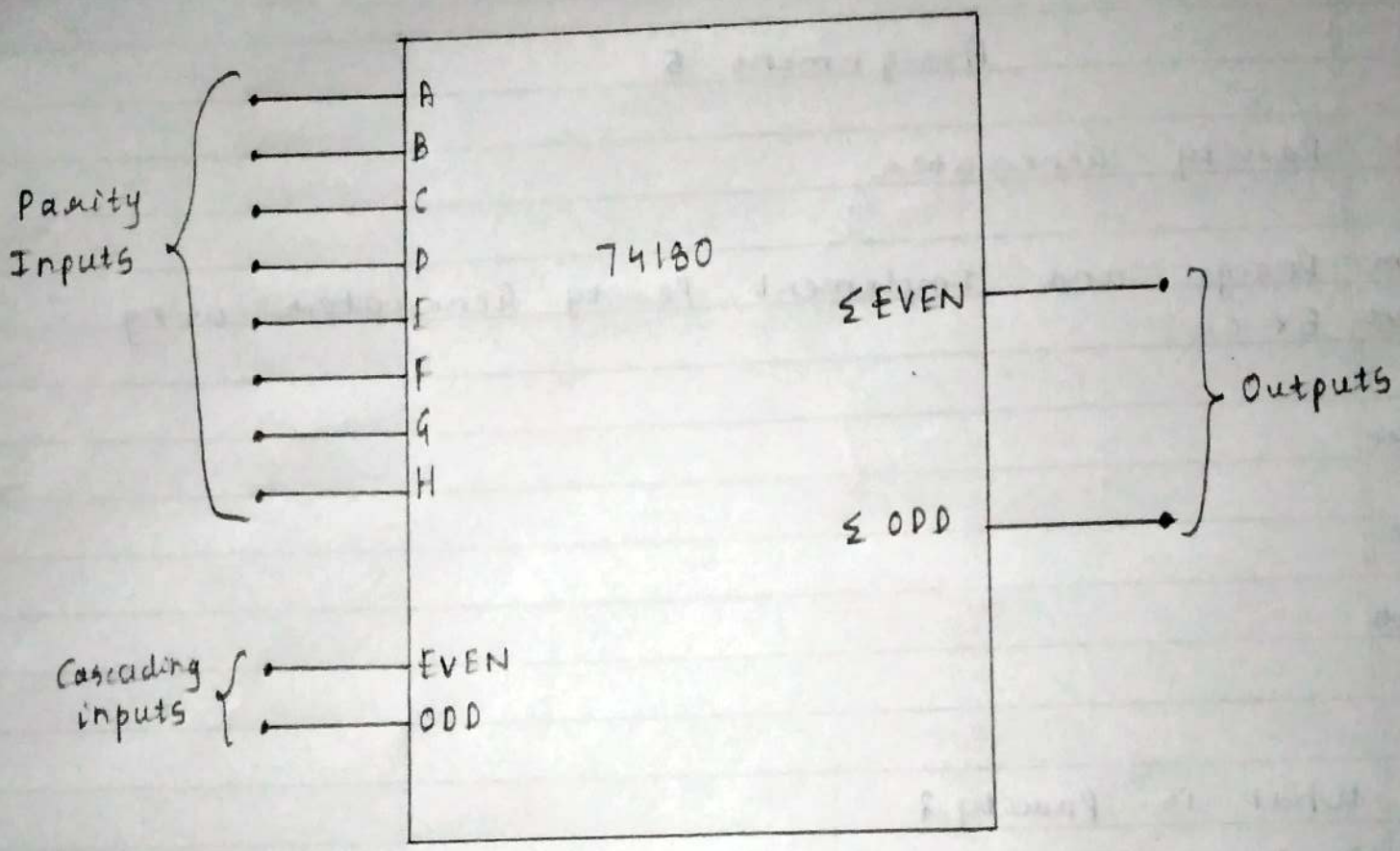
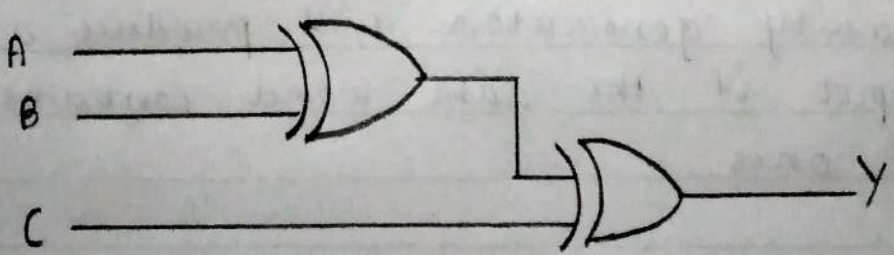
2) Parity Generator



→ Circuit diagram (Even parity Generator)



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Design:

1.

a. Even Parity Generator

- Truth table

3-bit message			Even parity bit generator (P)
A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

- K-map

Y / A \ BC	$\bar{B}\bar{C}$	$\bar{B}C$	BC	$B\bar{C}$
$\bar{A}$	0 (0)	1 (1)	0 (3)	1 (2)
A	1 (4)	0 (5)	1 (7)	0 (6)

$$Y = A\bar{B}\bar{C} + ABC + \bar{A}\bar{B}C + \bar{A}B\bar{C}$$
$$= A(\bar{B}\bar{C} + BC) + \bar{A}(\bar{B}C + B\bar{C})$$
$$= A(\overline{B \oplus C}) + \bar{A}(B \oplus C)$$
$$= A \oplus B \oplus C$$

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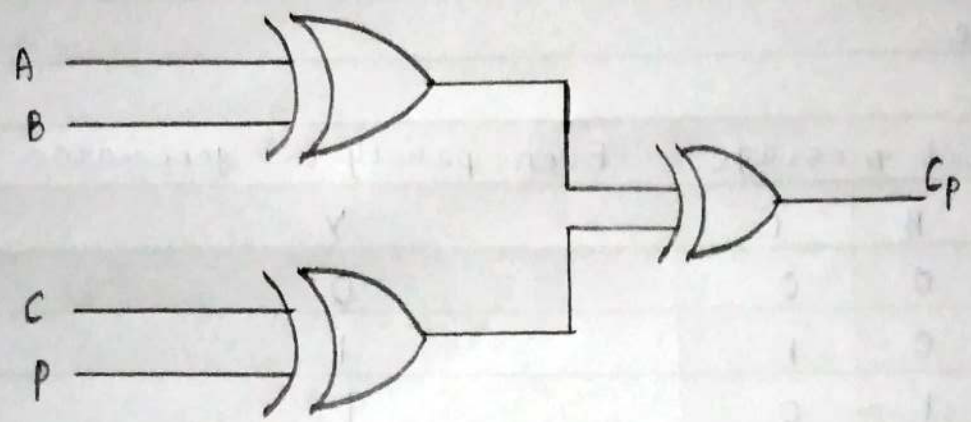
→ Circuit diagram (Even parity detector)



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b. Even parity checker / detector

- Truth table

4 bit received message				Parity Error Check C_p
A	B	C	P	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

- K-map

C_p : AB \ CP	$\bar{C}\bar{P}$	$\bar{C}P$	CP	$C\bar{P}$
$\bar{A}\bar{B}$	0 (0)	1 (1)	0 (3)	1 (2)
$\bar{A}B$	1 (4)	0 (5)	1 (7)	0 (6)
AB	0 (12)	1 (13)	0 (15)	1 (14)
$A\bar{B}$	1 (8)	0 (9)	1 (11)	0 (10)

$C_p = \bar{A}\bar{B}\bar{C}P + \bar{A}\bar{B}C\bar{P} + \bar{A}B\bar{C}\bar{P} + \bar{A}BCP + AB\bar{C}P + ABC\bar{P} + A\bar{B}\bar{C}\bar{P} + A\bar{B}CP$

$= \bar{A}\bar{B}(\bar{C}P + C\bar{P}) + \bar{A}B(\bar{C}\bar{P} + CP) + AB(\bar{C}P + C\bar{P}) + A\bar{B}(\bar{C}\bar{P} + CP)$

$= C(\overline{A \oplus P})(A \oplus B) + (C \oplus P)(\overline{A \oplus B})$

$\therefore C_p = A \oplus B \oplus C \oplus P$

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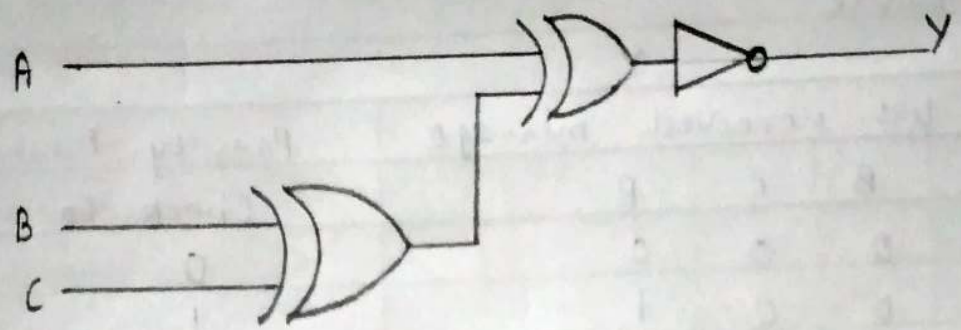
→ Circuit diagram Odd Parity Generator



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2. a. Odd Parity Generator

- Truth table

3-bit message			Odd Parity bit generator (P)
A	B	C	
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

- K-map Y

A \ BC	$\bar{B}\bar{C}$	$\bar{B}C$	BC	$B\bar{C}$
$\bar{A}$	1 (0)	0 (1)	1 (3)	0 (2)
A	0 (4)	1 (5)	0 (7)	1 (6)

$$Y = \bar{A}B\bar{C} + \bar{A}BC + A\bar{B}C + AB\bar{C}$$
$$= \bar{A}(B\bar{C} + BC) + A(\bar{B}C + B\bar{C})$$
$$= \bar{A}(\overline{B \oplus C}) + A(B \oplus C)$$
$$= A \odot (B \oplus C)$$

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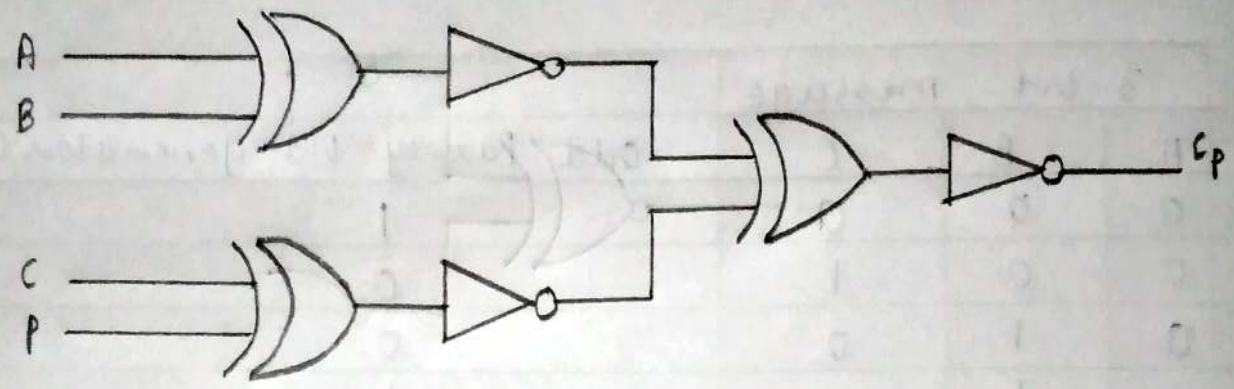
→ Circuit diagram of odd parity checker (4 bit)



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b Odd parity Detector

4-bit received message				Parity error check C_p
A	B	C	P	
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

- K-map

C_p \ CP / AB	$\bar{C}\bar{P}$	$\bar{C}P$	CP	$C\bar{P}$
$\bar{A}\bar{B}$	(1) 0	0 1	(1) 3	0 2
$\bar{A}B$	0 4	(1) 5	0 7	(1) 6
AB	(1) 12	0 13	(1) 15	0 14
$A\bar{B}$	0 8	(1) 9	0 11	(1) 10

$C_p = \bar{A}\bar{B}\bar{C}\bar{P} + \bar{A}\bar{B}CP + \bar{A}B\bar{C}P + \bar{A}BC\bar{P} + AB\bar{C}\bar{P} + ABCP + A\bar{B}\bar{C}P + A\bar{B}C\bar{P}$

$= \bar{A}\bar{B}(\bar{C}\bar{P} + CP) + \bar{A}B(\bar{C}P + C\bar{P}) + AB(\bar{C}\bar{P} + CP) + A\bar{B}(\bar{C}P + C\bar{P})$

$= C\overline{(\bar{C} \oplus P)}(\overline{A \oplus B}) + (C \oplus P)(A \oplus B)$

$C_p = (A \odot B) \odot (C \odot P)$

Conclusion: Designed and Implemented parity Generator using EX-OR.

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