Assignment No. 1.

Problem Statement : Study of Shift Registers (SISO, SIPO, PISO, PIPO).

Theory :-

The binary data in a register can be moved within the register from one flip-flop to the other or outside it with application of clock pulses.

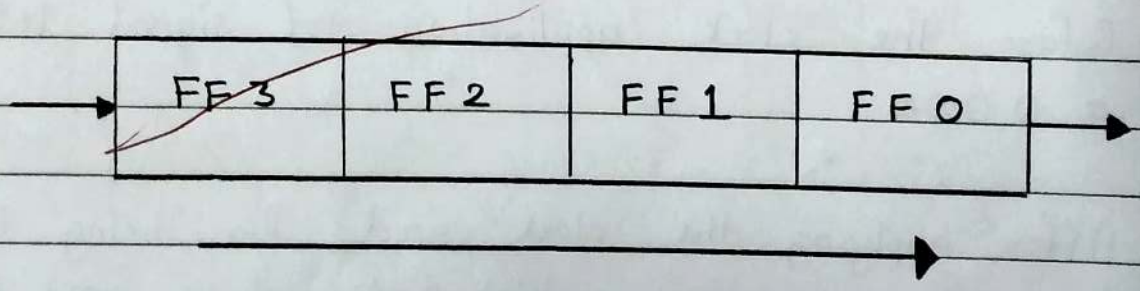
The registers that allow such data transfers are called as shift registers.

Shift registers are used for data storage, data transfer and certain arithmetic and logic operations.

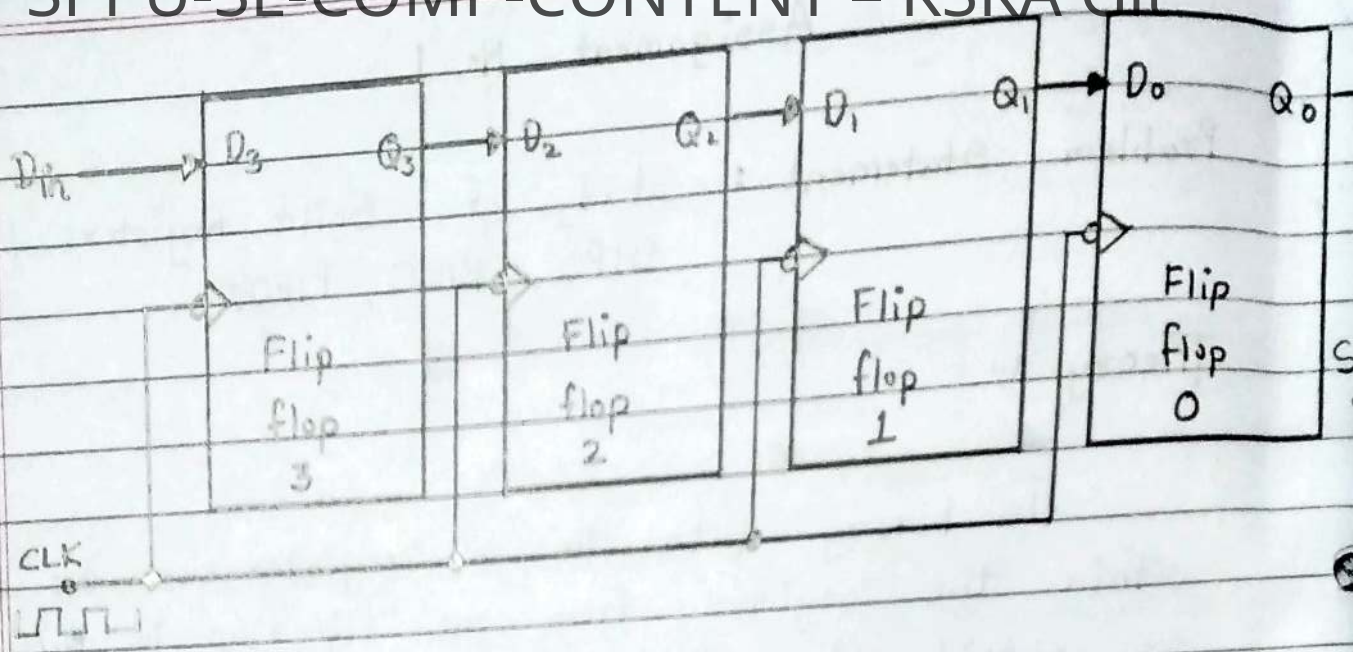
The various modes in which a shift register can operate are as follows :-

1. Serial Input Serial Output (SISO).

Data shifts from left to right by 1 position per clock cycle.



– Logic diagram :-



- Truth table :-

CLK	$D_{in} = D_3$	$Q_3 = D_2$	$Q_2 = D_1$	$Q_1 = D_0$	Q_0
Initially	–	0	0	0	0
↓ (1st)	1	1	0	0	0
↓ (2nd)	1	1	1	0	0
↓ (3rd)	1	1	1	1	0
↓ (4th)	1	1	1	1	1

- Operation :-

1. Before the clock application of signal let $Q_3\ Q_2\ Q_1\ Q_0$ = 0 0 0 0.

2. After applying the clock and Din being high i.e 1, the FF3 will produce high o/p while rest being low 0. i.e 1 0 0 0.

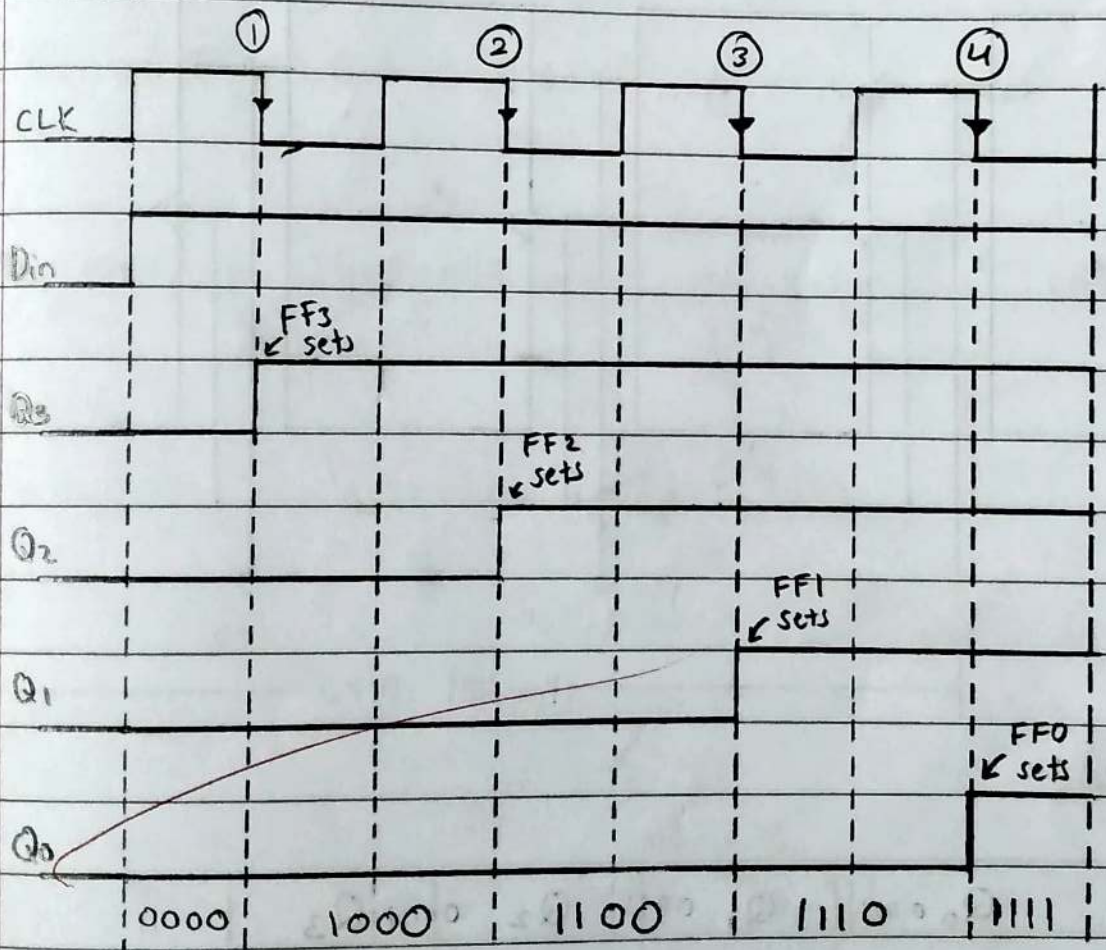
3. After the 2nd clock pulse, the FF2 will set and stored

word changes to, $Q_3 Q_2 Q_1 Q_0 = 1100$.

4. $D_{in} = 1$, as soon as the third negative clock edge gets applied, FF1 will be set and o/p gets modified to, $Q_3 Q_2 Q_1 Q_0 = 1 1 1 0$.

5. Similiarly with $D_{in} = 1$ and the forth clock pulse being applied, Stored word changes to:
$Q_3 Q_2 Q_1 Q_0 = 1 1 1 1$.

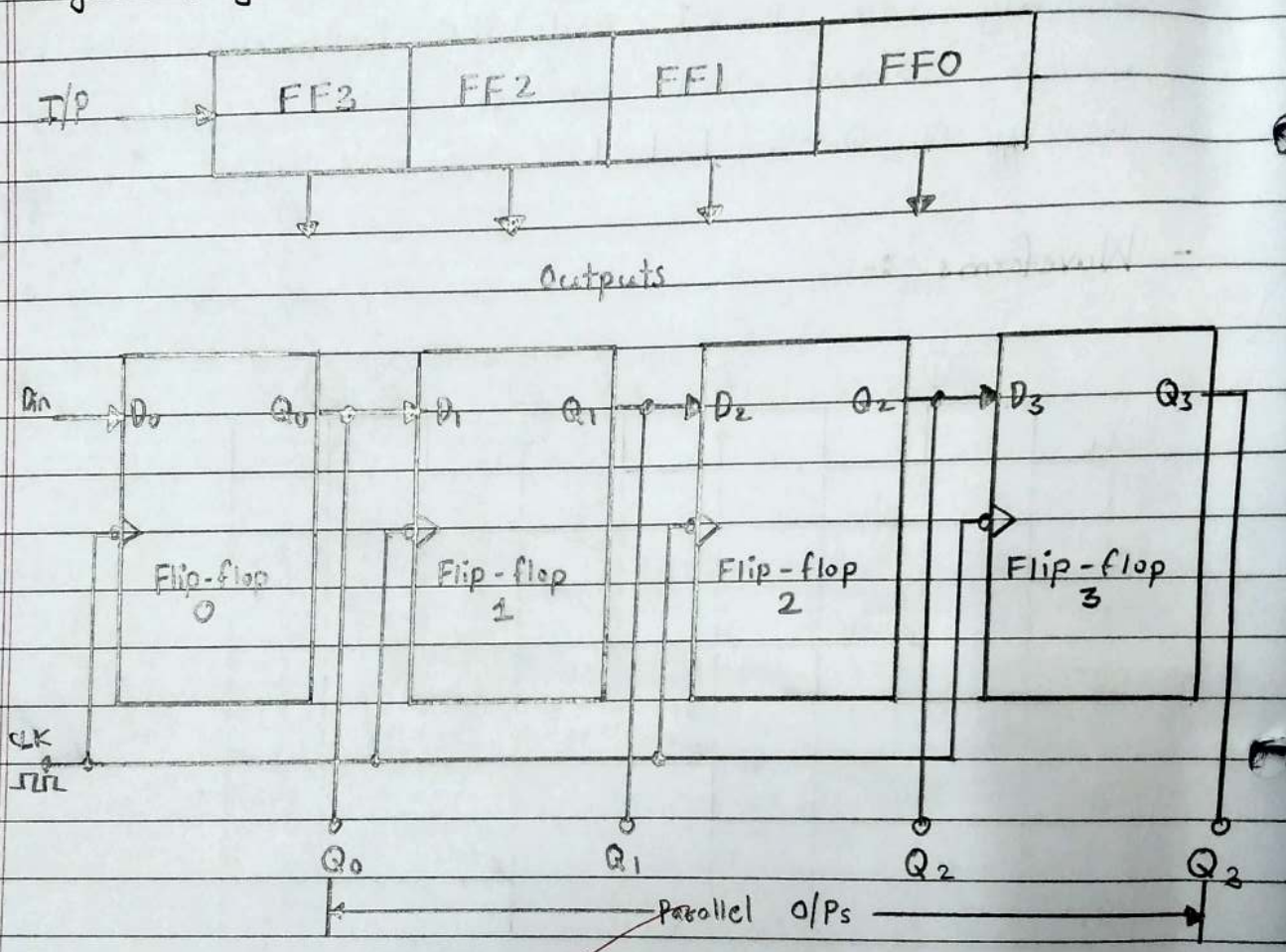
- Waveforms :-



2. Serial In Parallel Out (SIPO) :-

In this operation the data is entered serially and taken out in parallel as shown below :-

- Logic diagram :-



- Truth table :-

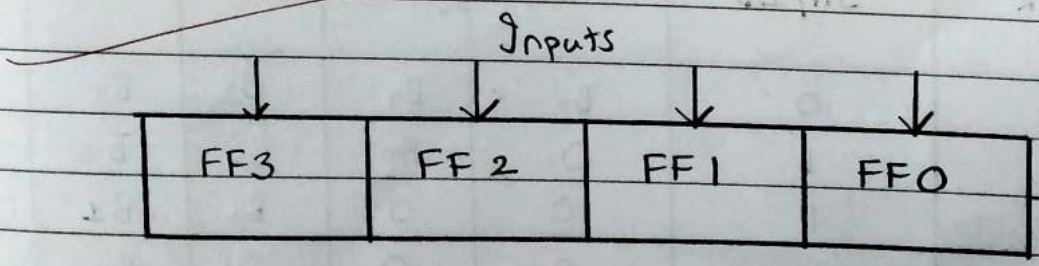
CLK	Q_0	Q_1	Q_2	Q_3
Initially	0	0	0	0
↓ (1st)	1	0	0	0
↓ (2nd)	1	1	0	0
↓ (3rd)	1	1	1	0
↓ (4th)	1	1	1	1

- Operation :-

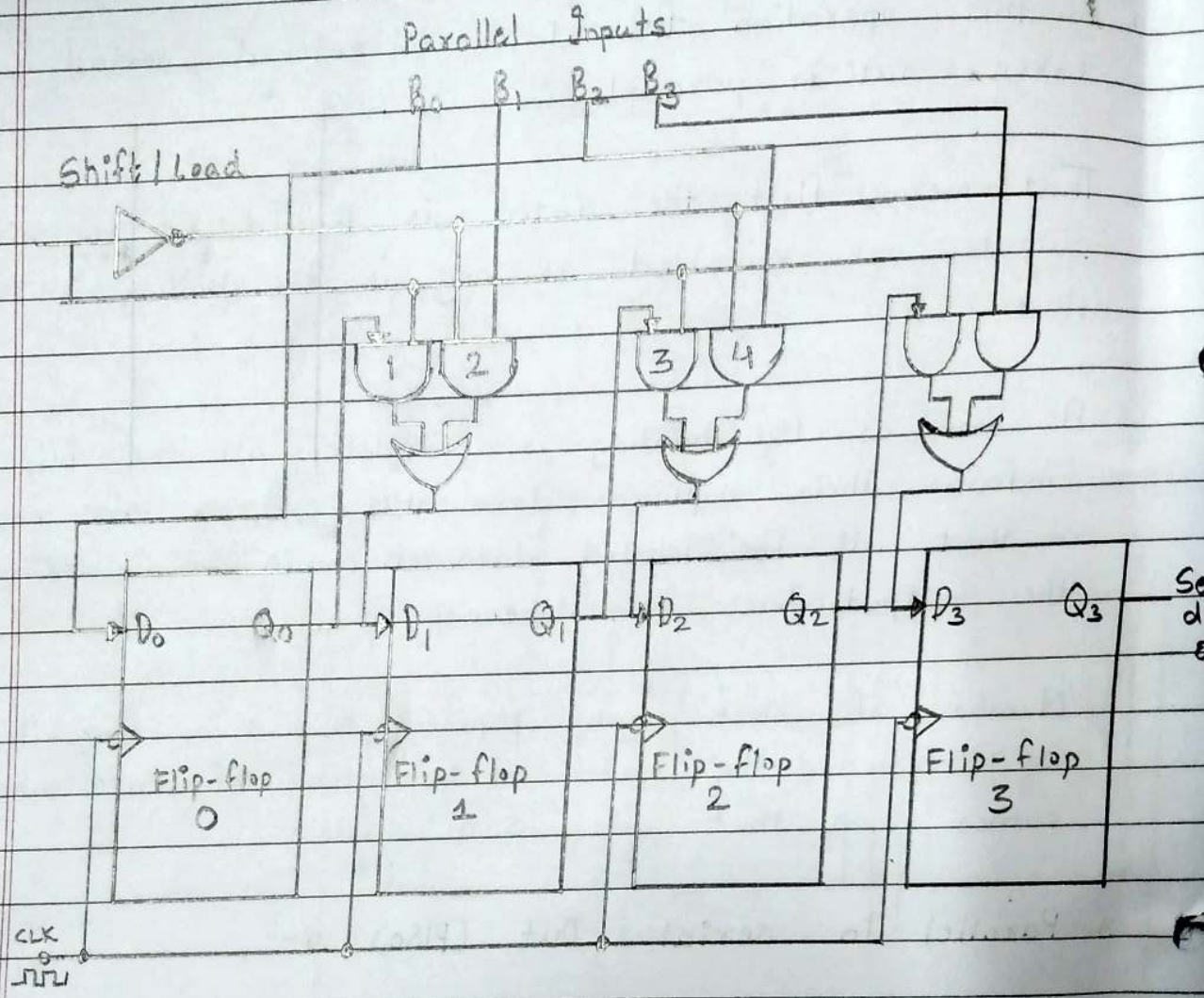
1. In this operation the data is entered serially and taken out in parallel
2. That means first the data is loaded bit by bit. The outputs are disabled as long as the loading is taking place.
3. As soon as the loading is complete, all the flip-flops contains their required data the outputs are enabled so that all the loaded data is made available over all the output lines simultaneously.
4. Number of clock cycles required to load a four bit word is 4. Hence the speed of operation of SIPO mode is sames as that of SISO mode.

3. Parallel In serial Out (PISO) :-

In this mode, the bits are entered in parallel i.e simultaneously into a shift register as shown below:



- Logic diagram :-



- Truth table :-

CLK	SH/LD	Q0	Q1	Q2	Q3	Data o/p
1	0	B_0	B_1	B_2	B_3	B_3
2	1	0	B_0	B_1	B_2	B_2
3	1	0	0	B_0	B_1	B_1
4	1	0	0	0	B_1	B_1
5	1	0	0	0	0	0

- Operation :-

1. In the PISO register, output of previous FF is connected to the input of the next one via a combinational ckt.

2. The binary input word B_0, B_1, B_2, B_3 is applied through the same combinational circuit.

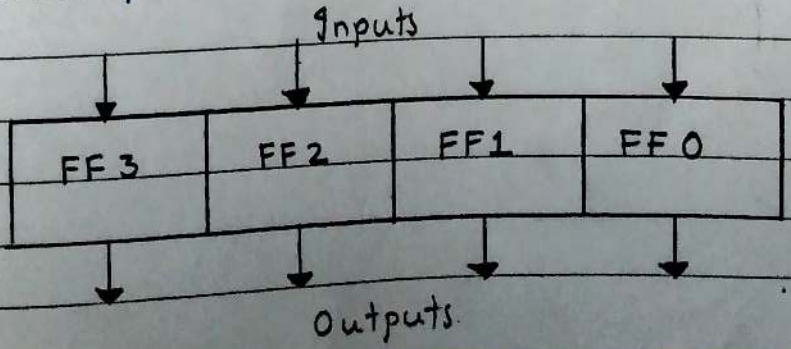
3. There are two modes in which this circuit can work namely shift mode or load mode.

a) Load mode: In order to load the word B_3, B_2, B_1, B_0 into the shift register, set shift/$\overline{\text{load}}$ to 0. This will active the AND gates 2, 4 and 6. Hence, inputs B_0, B_1, B_2, B_3 will be directly passed to the B_0, B_1, B_2, B_3 inputs of flip-flops.

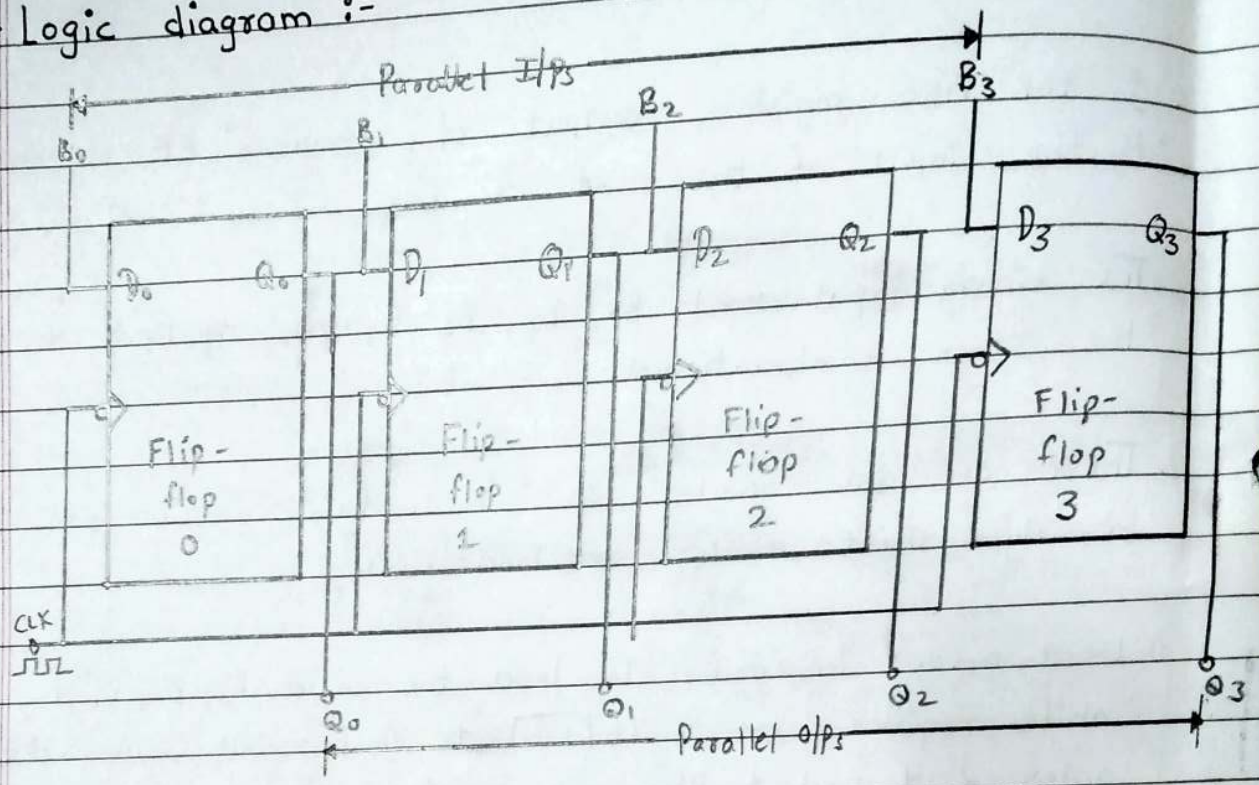
b) Shift mode: In order to use shift mode, apply logic 1 to the shift/$\overline{\text{load}}$ input. During shift mode, AND gates 2, 4, 6 become inactive. Thus the parallel in serial out operation takes place.

4. Parallel In Parallel Out (PIPO) :-

All inputs are loaded simultaneously and are available at the output simultaneously.



- Logic diagram :-



- Operation :-

1. When the negative clock edge is applied, the input binary bits will be loaded into the flip-flops simultaneously.

2. The loaded bits will appear simultaneously to the o/p side. Only one clock pulse is essential to load all the bits. Therefore, PIPO mode is the fastest mode of operation.

Conclusion: Hence, shift registers studied.

21/11/23