UNIT-III

ALGORITHMIC STATE MACHINES.

* Introduction to ASM :-

- As Algorithm is a step by step procedure g program or problem

whereas flowchart is graphical representation g algorithm.

Hence,

An ASM ([redacted] Algorithmic state machine) chart is Similar to the conventional flowchart but we interepret in different manner..

Def:- "ASM chart is basically a flowchart which represent hardware algorithm."

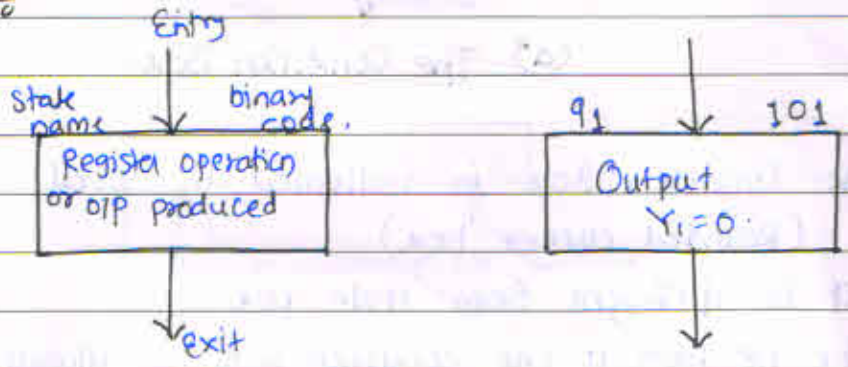
It is useful to design the h/w sequential ckt as per specification.

* ASM chart Notation :-

An ASM chart is composed g 3 basic elements.

1) The state box 2) The decision box 3) The condition box

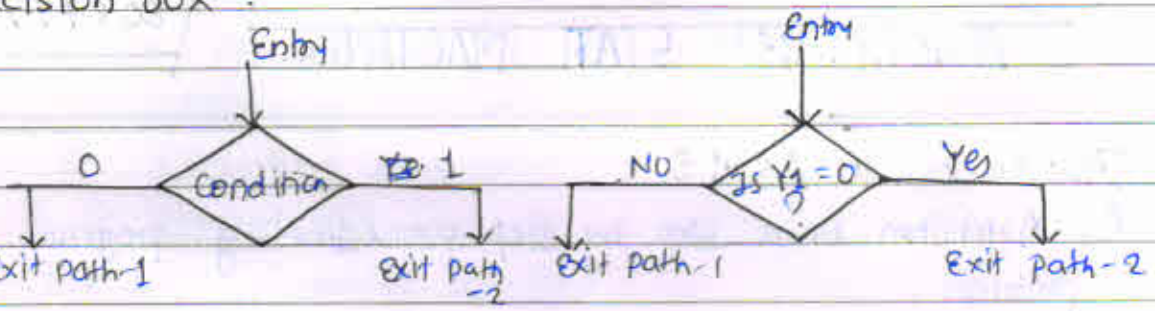
1) The state box :-



(a) General description (b) example g state Box.

- state box is used for indicating the state g the controller in the control sequence. as shown in fig.
- The state box is rectangular in shape.
- I/P to state box is indicated by 'entry'
  o/p to state box is indicated by 'exit'.

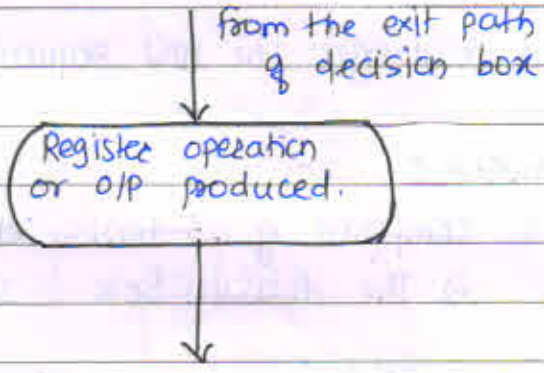
2) Decision Box :-



(a) General Description (b) Example.

- Decision box is indicated by diamond shape.
- It has two or more exit paths.
- Decision box is used to make Condition as per state.

3) Condition Box :-



(a) The Condition Box.

- The Condition Box is indicated by oval shape rectangle (Rounded corner box)
- It is different from state box.
- The I/P path to the condition box is always comes from one of the exit path of decision box.

* Draw an ASM chart and state table of a 2-bit up-down Counter having a mode control.

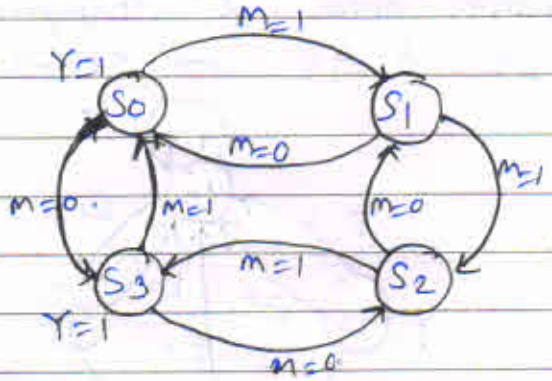
→ 1) Let mode control i/p be denoted by M.

M = 1 up Counting M = 0 Down Counting.

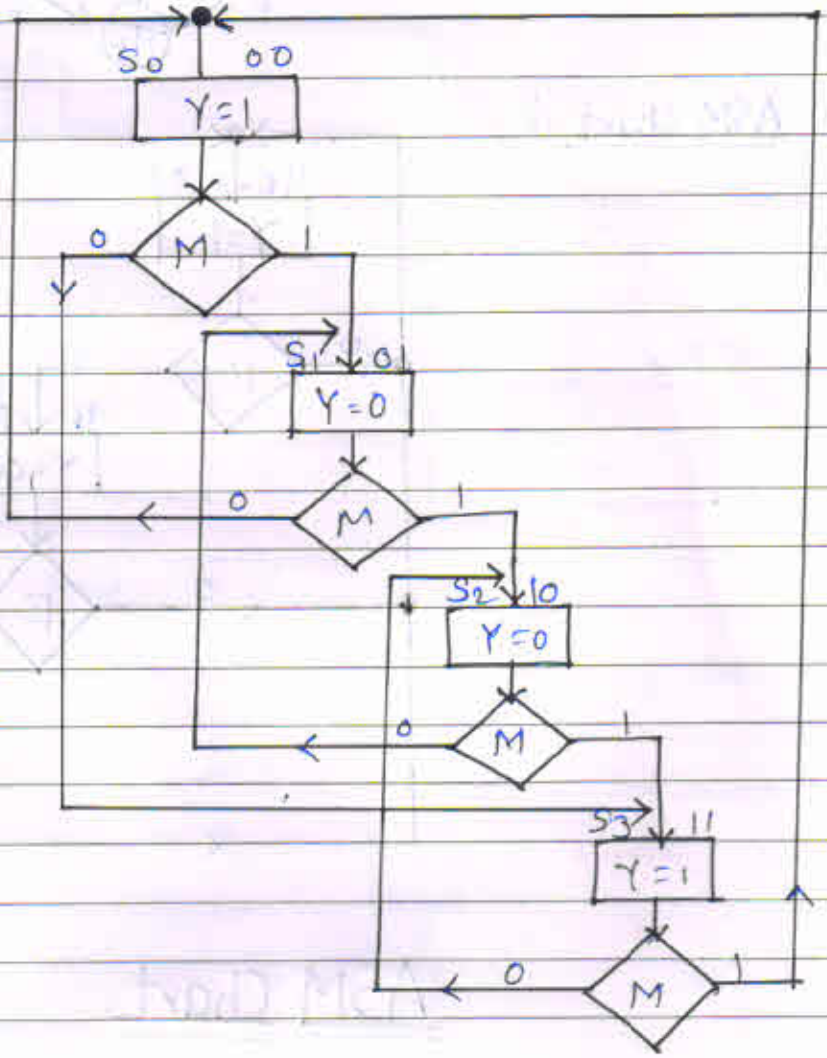
2) 2-bit require $2^2 = 4$ inputs state.

i.e. S_0, S_1, S_2 & S_3 → 00 → 01 → 10 → 11

3) State table :-



4) ASM Chart :-



2-Bit ASM Chart UP-DOWN Counter.

* Draw the ASM chart for a 2-bit binary Counter. having One enable line E. Such that.

E = 1 (Counting enabled)

E = 0 (Counting disabled)

→ 1) E is Control bit

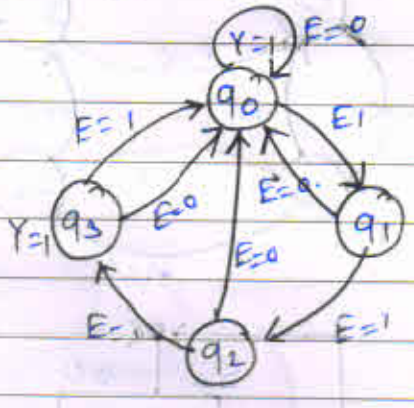
If E = 1 Counting Enabled

E = 0 Counting Disabled

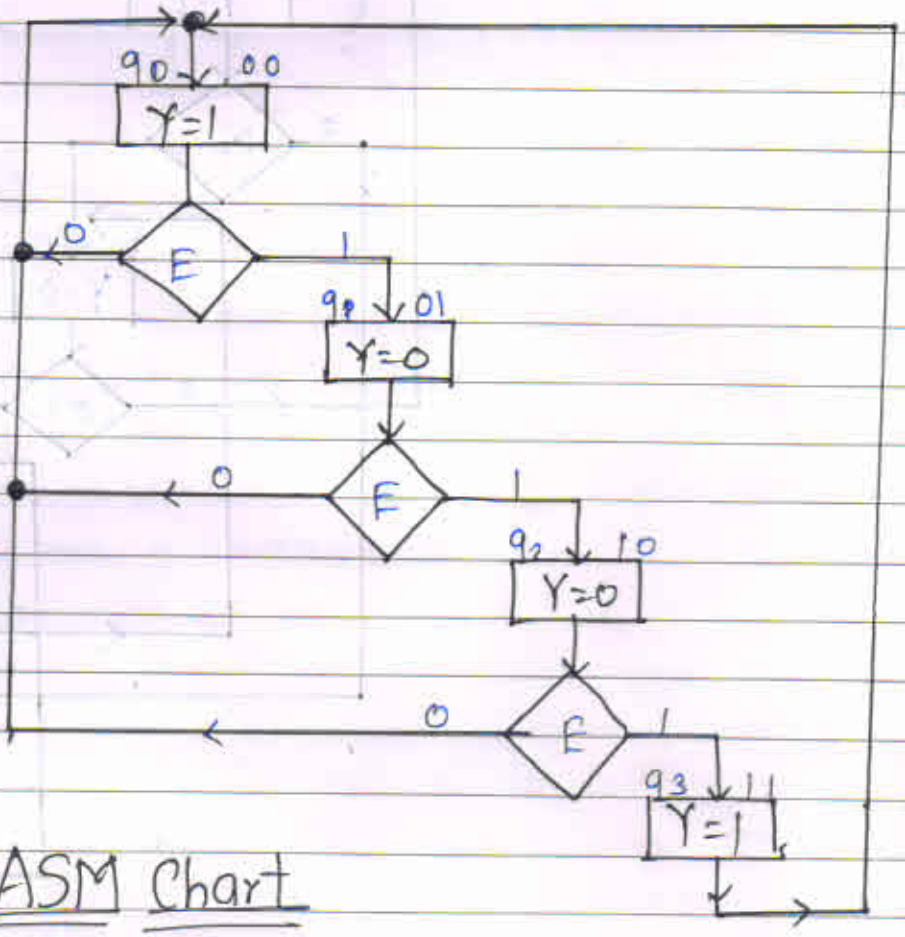
2) 2-bit binary counter needs $2^2 = 4$ input state.

q_0 , q_1 , q_2 & q_3 → 00 → 01 → 10 → 11

3) State table



4) ASM chart :



ASM Chart

* Draw the ASM Chart and state diagram for the synchronous circuit having the foll. description :

The circuit has control input 'C', clock & O/P x, y, z.

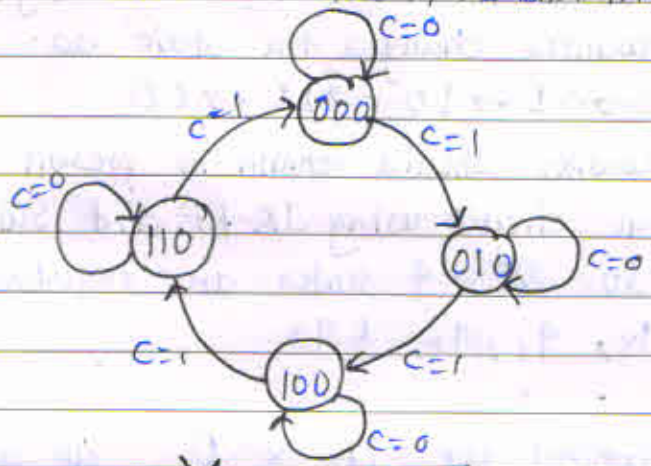
1. If C = 1, on every rising edge of clock code on O/P x, y & z changes from 000 → 010 → 100 → 110 → 000 and repeat.
2. If C = 0, then circuit holds the present state.

→ 1. There are 4-state so need 4 variable/state.

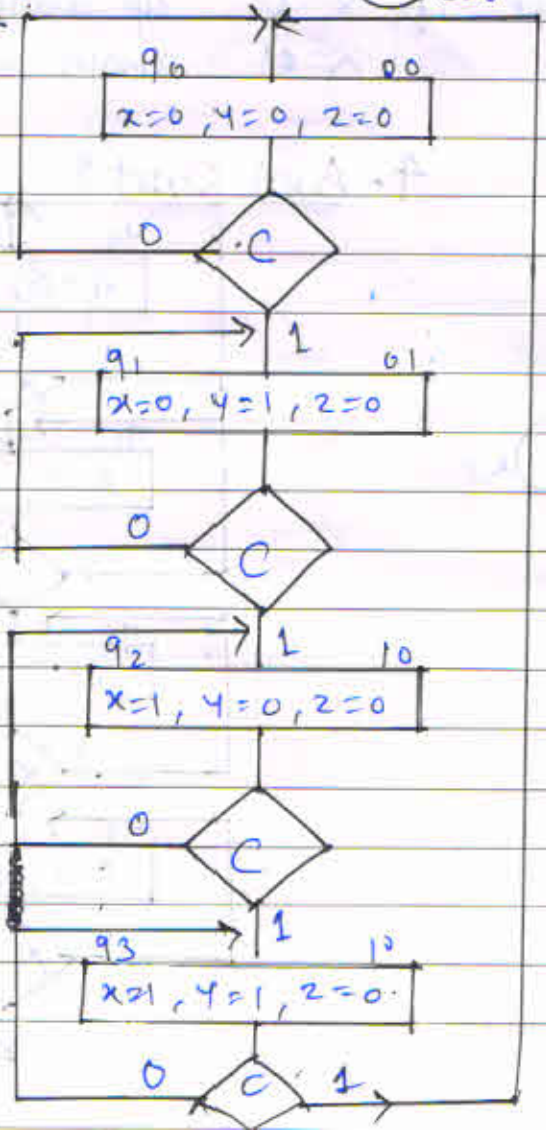
$q_0 = 00$, $q_1 = 01$, $q_2 = 10$ & $q_3 = 11$

2. C is control bit so If C = 1 then up counting
C = 0 then, remain in present state.

3. State diagram :



4. ASM chart :



* Multiplexer Input Condition :-

	Present state		Next state		I/P Condition	Multiplexer Input	
	S_1	S_0	S_1	S_0		MUX-1	MUX-2
q_0	0	0	0	1	No cond^n	$D_0 = 0$	$D_0 = 1$
q_1	0	1	1	0	No cond^n	$D_1 = 1$	$D_1 = 0$
q_2	1	0	1	1	No cond^n	$D_2 = 1$	$D_2 = 1$
q_3	1	1	0	0	No cond^n	$D_3 = 0$	$D_3 = 0$

0 0	→ 0
0 1	→ 1
1 0	→ 0
1 1	→ 1

* Draw the ASM chart for the foll. state machine; A two bit UP counter with o/p Q_1Q_0 and enable signal 'X' is to be designed

If 'x' = 0, counter changes the state as:

$00 \rightarrow 01 \rightarrow 10 \rightarrow 11 \rightarrow 00$

If x = 1, Counter should remain in present state.

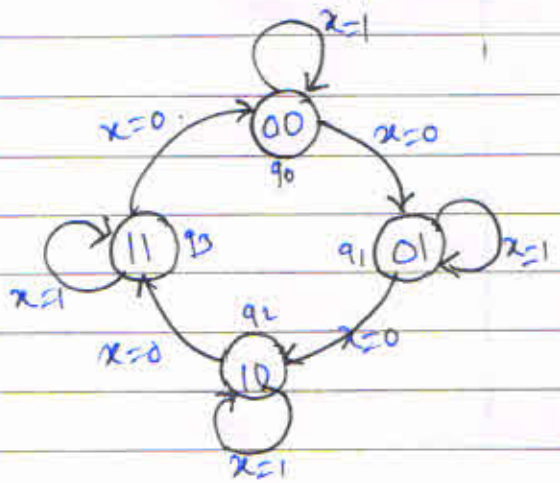
Design your circuit using JK-FF and suitable MUX.

→ 1. 2-bit so $2^2 = 4$ states are required.

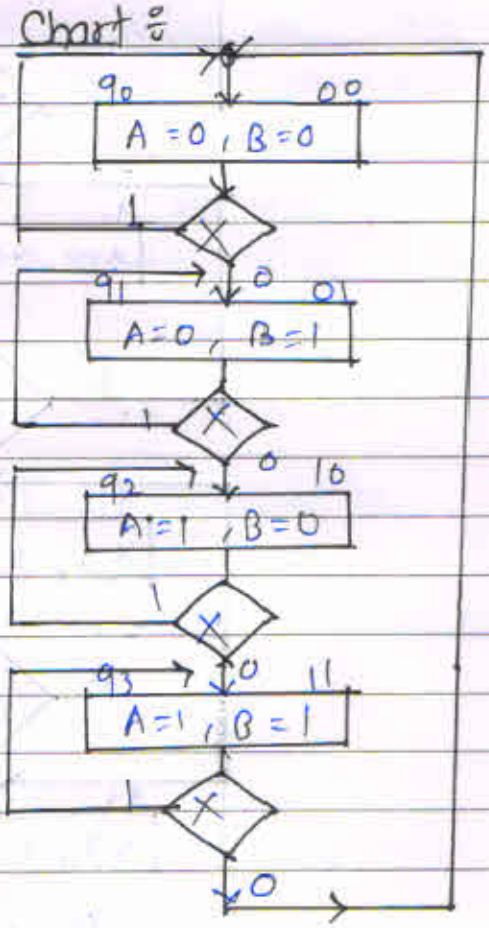
PART-I q_0, q_1, q_2 & q_3

2. X is control bit If X=0 up counting.
X=1 remain in present state.

3. State diagram :-



4. ASM Chart :-

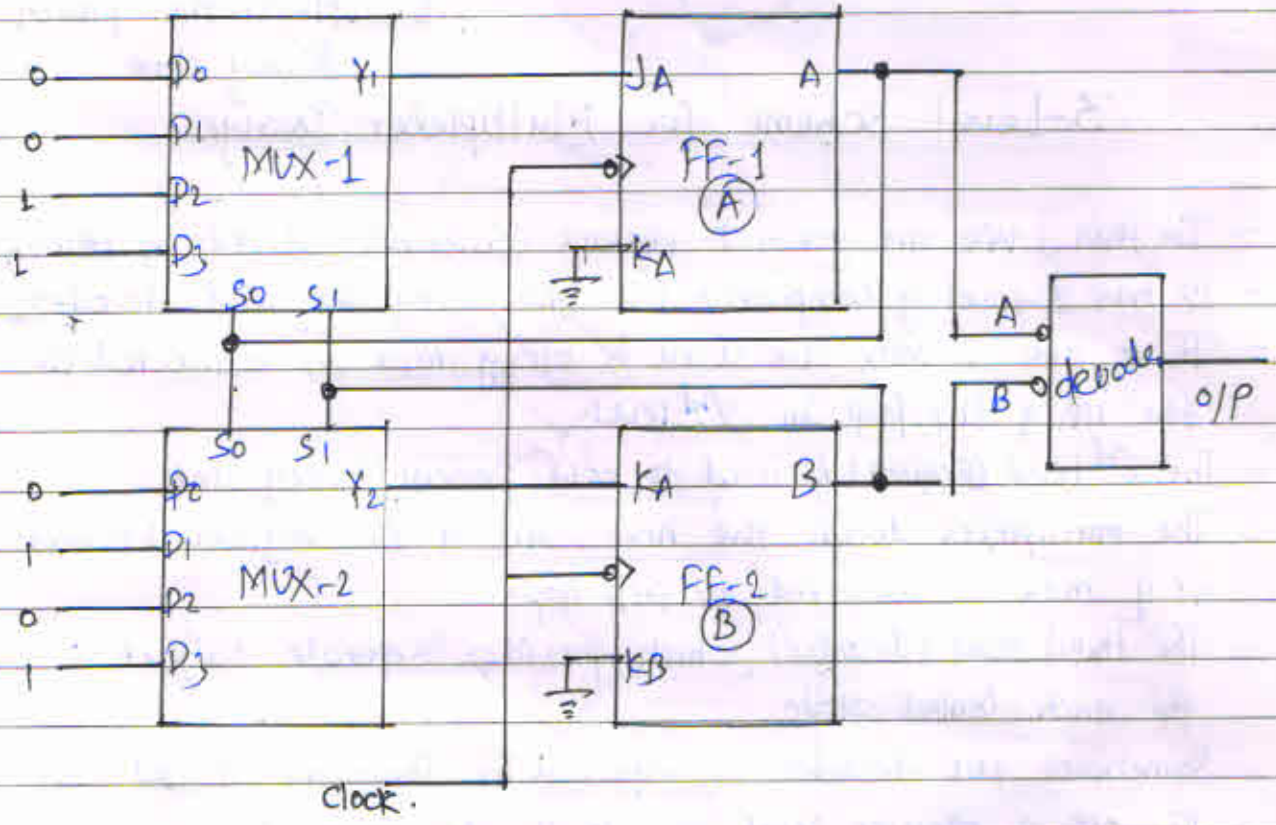


PART-II MUX Controller Method.

* Write table for MUX.

Present state.		Next state.		Input	MUX Input.	
S_1	S_0	S_1	S_0	X	MUX-1	MUX-2
0	0	0	1	0	$D_0 = 0$ } $D_0 = 0$	$D_0 = 1$ } $D_0 = 0$
0	0	0	0	1	$D_0 = 0$ }	$D_0 = 0$ }
0	1	1	0	0	$D_1 = 1$ } $D_1 = 0$	$D_1 = 0$ } $D_1 = 1$
0	1	0	1	1	$D_1 = 0$ }	$D_1 = 1$ }
1	0	1	1	0	$D_2 = 1$ } $D_2 = 1$	$D_2 = 1$ } $D_2 = 0$
1	0	1	0	1	$D_2 = 1$ }	$D_2 = 0$ }
1	1	0	0	0	$D_3 = 0$ } $D_3 = 1$	$D_3 = 0$ } $D_3 = 1$
1	1	1	1	1	$D_3 = 1$ }	$D_3 = 1$ }

* Draw the Logic diagram :-



Realization Using JK-FF And Multiplexer.

* MUX Controller Method :- (Design with Multiplexer)

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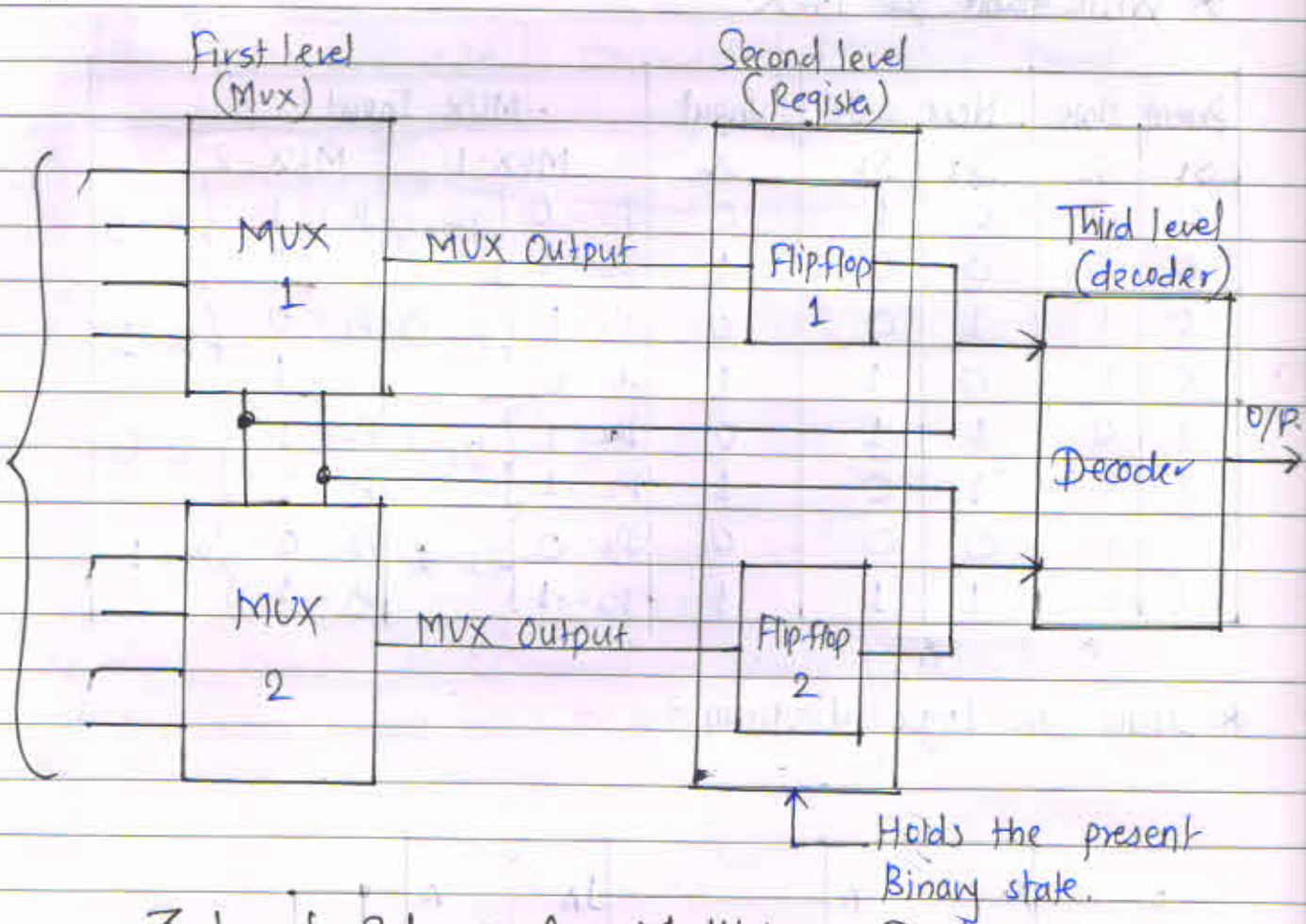

3-Level Scheme for Multiplexer Design.

- In this, We are going to replace combinational ckt by Multiplexer.
- It has 3-level of Component i.e. MUX, register and decoder.
- There are 2-MUX are used & o/p of mux is connected to the i/p of flip-flop in 2nd level
- The 2nd level (Register) is used to hold present binary state.
- The multiplexer decide the next state of the register because o/p of mux is connected to flip-flop.
- The third level (decoder), which provides seperate output for each control state.
- Sometimes the decoder is replaced by Combinational ckt.
- The o/p of register level is i/p to the decoder.
- This is the basic Concept to ~~con~~ understand MUX controller.