What is Programmable Logic Array (PLA)?

Programmable Logic Array (PLA) is a type of device which comes from the class of programmable logic devices (PLDs) and is used to implement combinational circuits. The basic configuration of a PLA consists of a programmable AND gate followed by a programmable OR gate. Although PLA contains the word programmable inside it, it does not have to be programmed explicitly using any programming languages like C, C++, Java, Python, etc.

A schematic diagram of the basic configuration of PLAs can be drawn as:

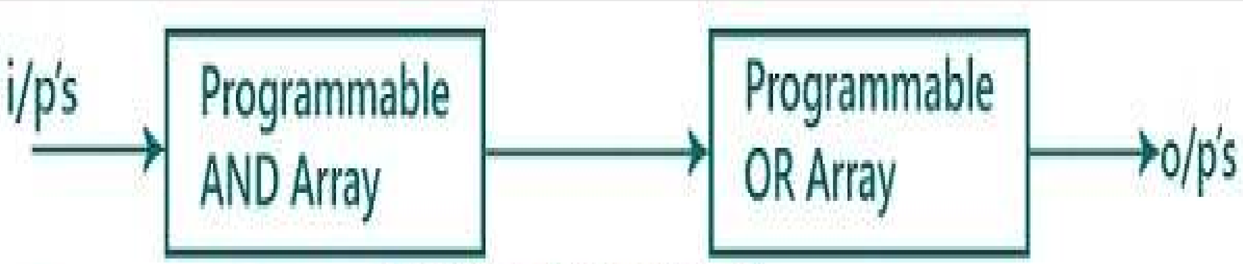


Fig:- Basic configuration of Programmable logic array.

Programmable Logic Array (PLA) Examples

Example 1

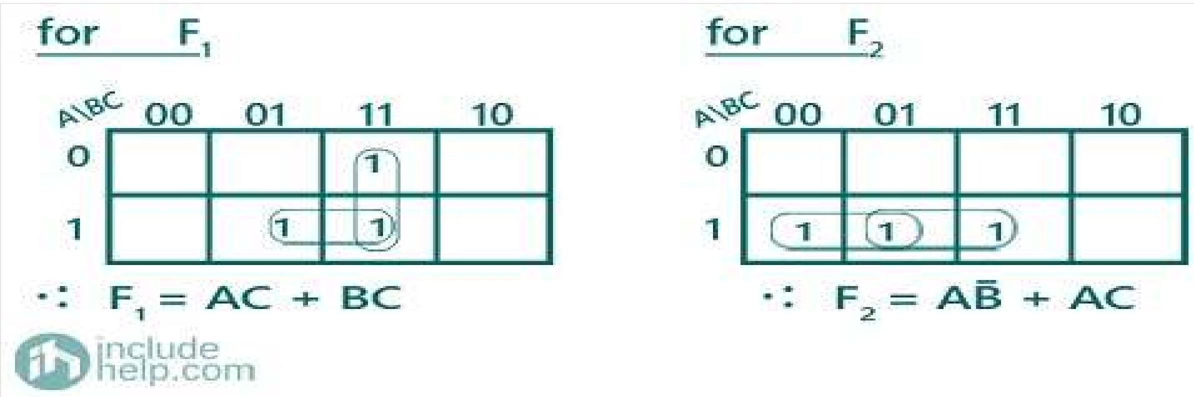
A combinational circuit is defined by the function F1= ∑ m (3,5,7), F2 = ∑ m (4,5,7). Implement the circuit using a PLA which consists of 3 inputs (A, B and C), 3 product terms and two outputs.

Solution

Since, F1= ∑ m (3,5,7) and F2 = ∑ m (4,5,7). Truth table for Boolean functions F1 and F2 can be drawn as:

Inputs			Outputs	
A	B	C	F1	F2
0	0	0	0	0
0	0	1	0	0
0	1	0	0	0
0	1	1	1	0
1	0	0	0	1
1	0	1	1	1
1	1	0	0	0
1	1	1	1	1

Now, for these Boolean functions, using the K-Map we can find the simplified Boolean expressions as:



A PLA program table can be also drawn representing the terms in the Boolean expression as:

PLA Program table :-

	Product term	i/P'S A	B	C	o/P'S F_1	F_2
1	AC	1	-	1	1	1
2	BC	-	1	1	1	-
3	AB	1	0	-	-	1

no . of i/P'S ⟶ 3
no. of Product terms ⟶ 3
no . of o/P'S ⟶ 2

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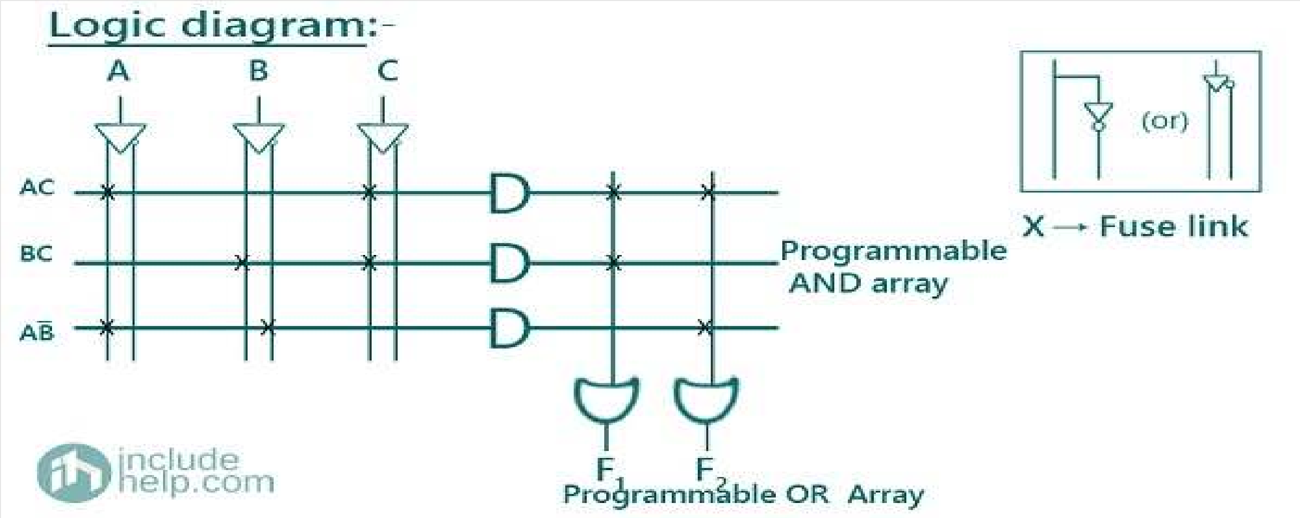
The logic diagram of the combinational circuit implemented using PLA can be drawn as:



Example 1

Design a BCD to Excess-3 code converter and implement it using a suitable PLA.

Solution

Truth table for BCD to Excess-3 converter can be drawn as:

Input (BCD Code)				Output (Excess-3 Code)			
B_3	B_2	B_1	B_0	E_3	E_2	E_1	E_0
0	0	0	0	0	0	1	1
0	0	0	1	0	1	0	0
0	0	1	0	0	1	0	1
0	0	1	1	0	1	1	0
0	1	0	0	0	1	1	1
0	1	0	1	1	0	0	0
0	1	1	0	1	0	0	1
0	1	1	1	1	0	1	0
1	0	0	0	1	0	1	1
1	0	0	1	1	1	0	0

Note: Since, BCD numbers are from 0-9, hence other combinations representing (10-15) are considered as don’t cares while solving the K-Map.

Boolean Expressions for all the outputs can be written as:

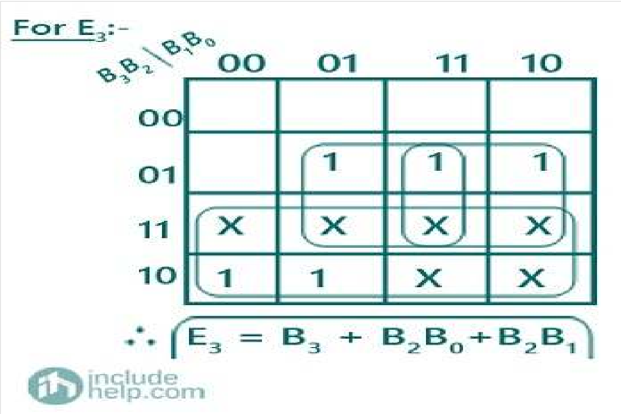
$E_3 = \sum m\ (5,6,7,8,9) + \sum d\ (10,11,12,13,14,15)$

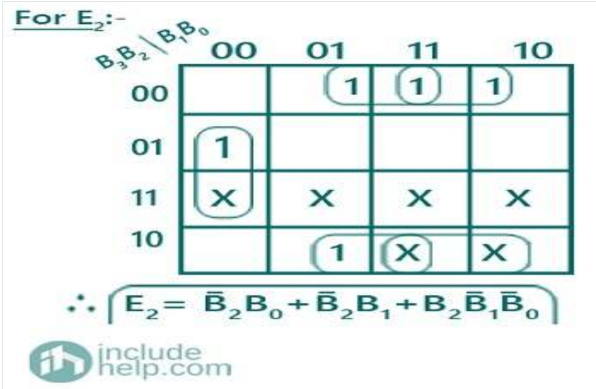
$E_2 = \sum m\ (1,2,3,4,9) + \sum d\ (10,11,12,13,14,15)$

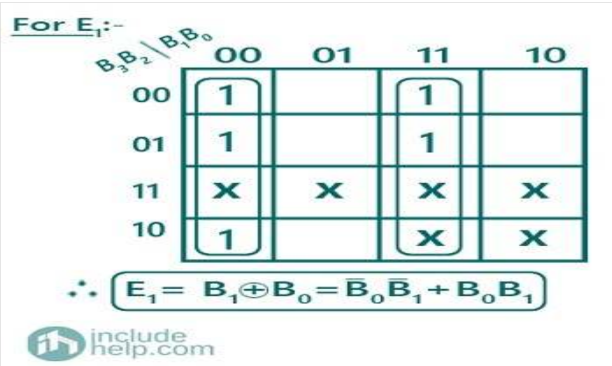
$E_1 = \sum m\ (0,3,4,7,8) + \sum d\ (10,11,12,13,14,15)$

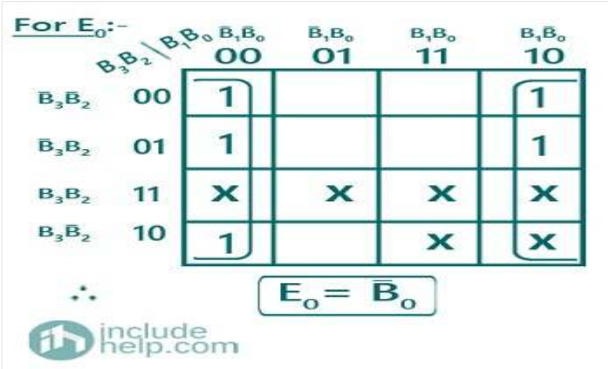
$E_0 = \sum m\,(0,2,4,6,8) + \sum d\,(10,11,12,13,14,15)$

Solving K-Map to get the required Boolean expressions:









A PLA program table can be also drawn representing the terms in the Boolean expression as:

PLA program table:-

Product terms	Inputs B_3	B_2	B_1	B_0	Outputs E_3	E_2	E_1	E_0
B_3	1	–	–	–	1	–	–	–
B_2B_0	–	1	–	1	1	–	–	–
B_2B_1	–	1	1	–	1	–	–	–
$\bar{B}_2B_0$	–	0	–	1	–	1	–	–
$\bar{B}_2B_1$	–	0	1	–	–	1	–	–
$B_2\bar{B}_1\bar{B}_0$	–	1	0	0	–	1	–	–
$\bar{B}_1\bar{B}_0$	–	–	0	0	–	–	1	–
B_1B_0	–	–	1	1	–	–	1	–
B_0	–	–	–	0	–	–	–	1

The logic diagram of the combinational circuit implemented using PLA can be drawn as: