

# SPPU-SE-COMP-CONTENT – KSKA Git

Total No. of Questions : 6]

SEAT No. :

P-5397

[Total No. of Pages : 2

[6186]-523

S.E. (Computer Engineering) (Insem.)

DIGITAL ELECTRONICS AND LOGIC DESIGN

(2019 Pattern) (Semester - III) (210245)

Time : 1 Hour]

[Max. Marks : 30

Instructions to the candidates :

- 1) Attempt Q.1 or Q.2, Q.3 or Q.4, Q.5 or Q.6.
- 2) Neat diagrams must be drawn wherever necessary.
- 3) Assume suitable data, if necessary.

Q1) a) Simplify the following function  $F(A, B, C, D) = \sum m(0, 2, 4, 5, 6, 7, 8, 10, 13, 15)$ . [5]

b) Simplify the following function [5]  
 $F(A, B, C, D) = \pi m(0, 2, 3, 8, 9, 12, 13, 15)$

OR

Q2) a) Simplify the following function  $F(A, B, C, D) = \sum m(0, 2, 4, 5, 6, 8, 10, 15) + d(7, 13, 14)$  [5]

b) Simplify the following function [5]  
 $F(w, x, y, z) = \sum m(4, 5, 7, 12, 14, 15) + d(3, 8, 10)$

Q3) a) Draw and explain 4-bit BCD adder using IC 7483. Explain any two BCD addition operations. [5]

b) Design a 4 bit Gray to Binary code converter? State the application of Gray code. [5]

OR

Q4) a) Design a 4 bit BCD to Excess-3 code converter circuit using logic gates. [5]

b) What is Multiplexer? Design 8:1 multiplexer with a dual 4:1 - multiplexer. [5]

P.T.O.

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- Q5) a)** What do you mean by half adder and full adder? How will you implement full adder using half adder? Draw the circuit diagram. [5]
- b) Convert the following expressions into their standard SOP form [5]
- i)  $Y = AB + AC + BC$
- ii)  $Y = A + BC + ABC$

OR

- Q6) a)** Minimize the function using K-map and implement Using NAND gates,  $F(A, B, C, D) = \sum m(4, 5, 6, 7, 8, 12) + d(1, 2, 3, 9, 11, 14)$ . [5]
- b) Write a short note on 2 bit comparator? [5]

