Assignment No. 5.

Title :- Sequence Generator.

Problem Statement :- Design and implement Sequence genator using J-K flip-flop.

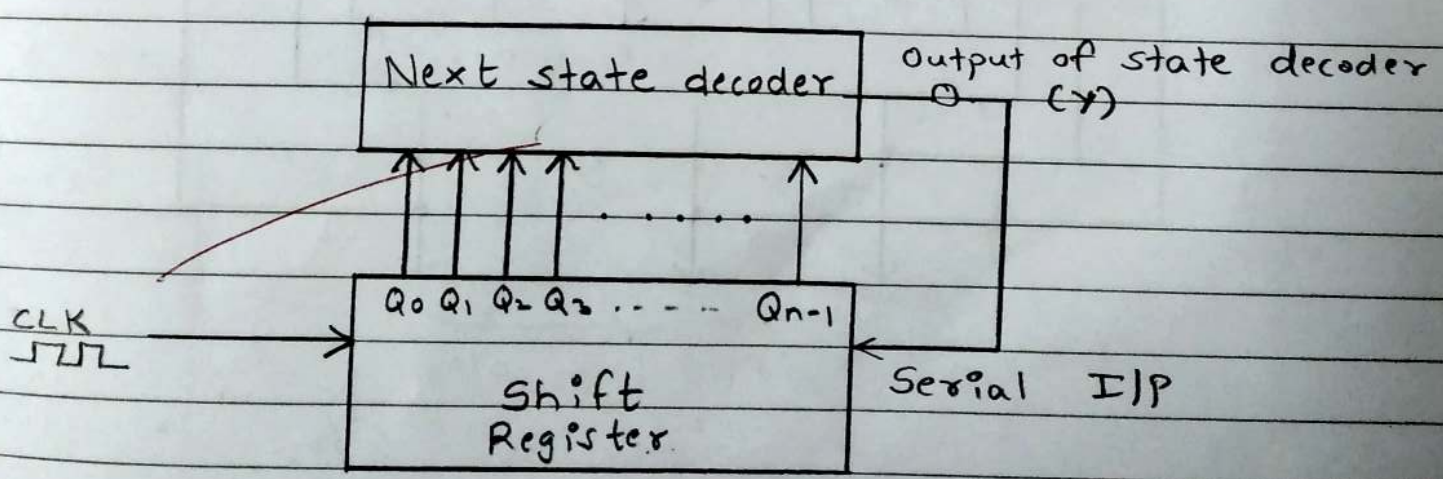
Hardware and Software requirements :-

Theory :-

Introduction to Sequence Generator :-

A sequence generator is a sequential circuit which generates the prescribed sequence at its output. The output sequence is produced in synchronization with the clock input.

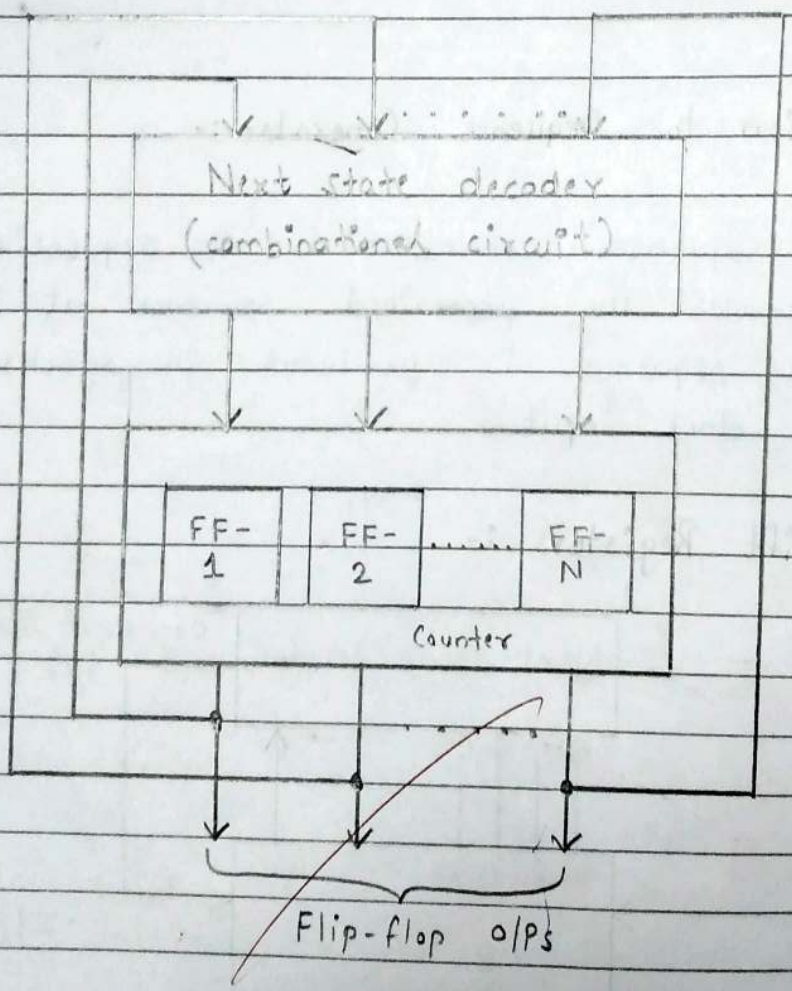
- Using Shift Registers :-



Basic structure of a sequence generator using shift registers.

The output of an N-bit shift register are applied as inputs to a combinational circuit called 'Next state decoder'.
And the output (Y) of the next state decoder is applied as a serial input to the shift register.
The "Next state decoder" is designed by keeping in mind that of the required sequence.

- Using Counters :-



Block diagram of a sequence generator using counters.

The input to the next state decoder are obtained from the flip-flops outputs and its output are applied to the input of the flip-flops.

Design :-

Design and implement Sequence generator using J-K flip flop for following sequence 1001001 using Counter.

1. Decide the no. of FF :

No. of 1's = 3 ∴ N = 4.
No. of 0's = 4

∴ Let n be the no. of flip-flops required,

∴ $N \leq 2^{n-1} \equiv 4 \leq 2^{n-1}$

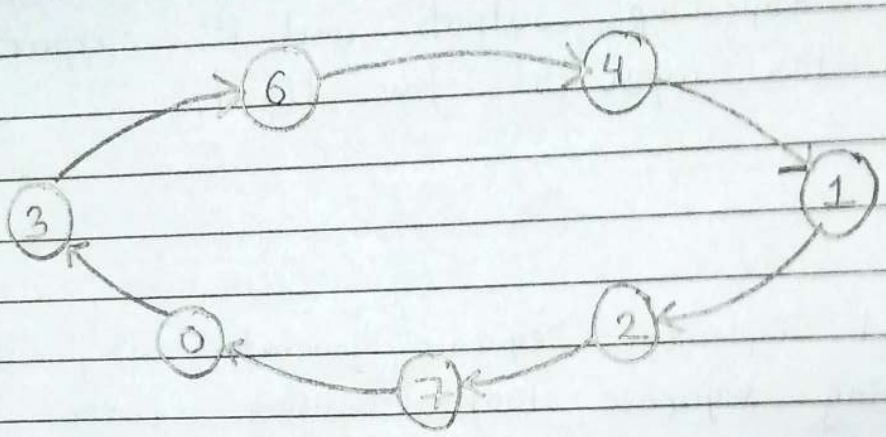
∴ n = 3.

So three FFs will be required.

2. Write the state table :-

Q_2	Q_1	Q_0	State
1	0	0	4
0	0	1	1
0	1	0	2
1	1	1	7
0	0	0	0
0	1	1	3
1	1	0	6

3. State diagram :-



4. Write excitation table :-

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	0
1	0	X	1
1	1	X	0

Present state			Next State			Flip-flop Inputs					
Q_2	Q_1	Q_0	Q_{2+1}	Q_{1+1}	Q_{0+1}	J_2	K_2	J_1	K_1	J_0	K_0
0	0	0	0	1	1	0	X	1	X	1	X
0	0	1	0	1	0	0	X	1	X	X	1
0	1	0	1	1	1	1	X	X	0	1	X
0	1	1	1	1	0	1	X	X	0	X	1
1	0	0	0	0	1	X	1	0	X	1	X
1	0	1	X	X	X	X	X	X	X	X	X
1	1	0	1	0	0	X	0	X	1	0	X
1	1	1	0	0	0	X	1	X	1	X	1

← The next state and FFs are don't care.

4. K-Map :-

For J_2 :-

Q_2 \ Q_1Q_0	00	01	11	10
0	0 (0)	0 (1)	1 (3)	1 (2)
1	X (4)	X (5)	X (7)	X (6)

$\therefore J_2 = Q_1$

For K_2 :-

Q_2 \ Q_1Q_0	00	01	11	10
0	X (0)	X (1)	X (3)	X (2)
1	1 (4)	X (5)	1 (7)	0 (6)

$\therefore K_2 = \overline{Q_1} + Q_0.$

For J_1 :-

Q_2 \ Q_1Q_0	00	01	11	10
0	1 (0)	1 (1)	X (3)	X (2)
1	0 (4)	X (5)	X (7)	X (6)

$\therefore J_1 = \overline{Q_2}$

For K_1 :-

Q_2 \ Q_1Q_0	00	01	11	10
0	X (0)	X (1)	0 (3)	0 (2)
1	X (4)	X (5)	1 (7)	1 (6)

$\therefore K_1 = Q_2$

For J_0 :-

Q_2 \ Q_1Q_0	00	01	11	10
0	1 (0)	X (1)	X (3)	1 (2)
1	1 (4)	X (5)	X (7)	0 (6)

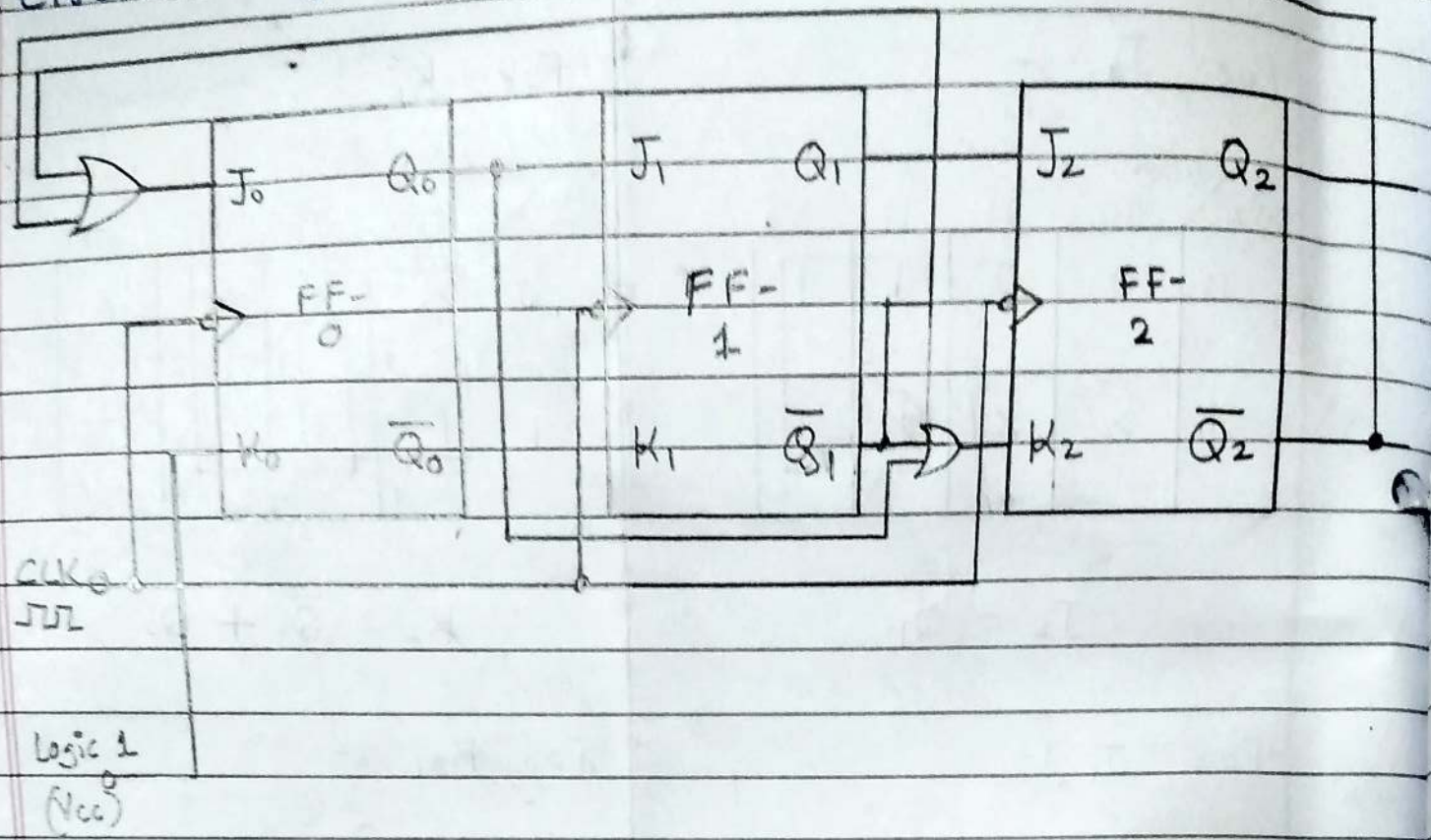
$\therefore J_0 = \overline{Q_2} + \overline{Q_1}$

For K_0 :-

Q_2 \ Q_1Q_0	00	01	11	10
0	X (0)	1 (1)	1 (3)	X (2)
1	X (4)	X (5)	1 (7)	X (6)

$\therefore K_0 = 1 \ (V_{cc})$

6. Circuit diagram :-



Conclusion :- Hence sequence generator studied.