

# SPPU-SE-COMP-CONTENT - KSKA Git

## Assignment No. 3

Title : a. Synchronous Counter.

Problem Statement : a. Realization of 3 bit UP/DOWN Counter using JK Flip-flops.

Hardware and Software requirements :

Theory :

Synchronous Counter :

In these counters all the flip-flops receive the external clock pulse is applied to all the flip-flops simultaneously.

Ring counter and Johnson counter are the examples of synchronous counters.

Design :-

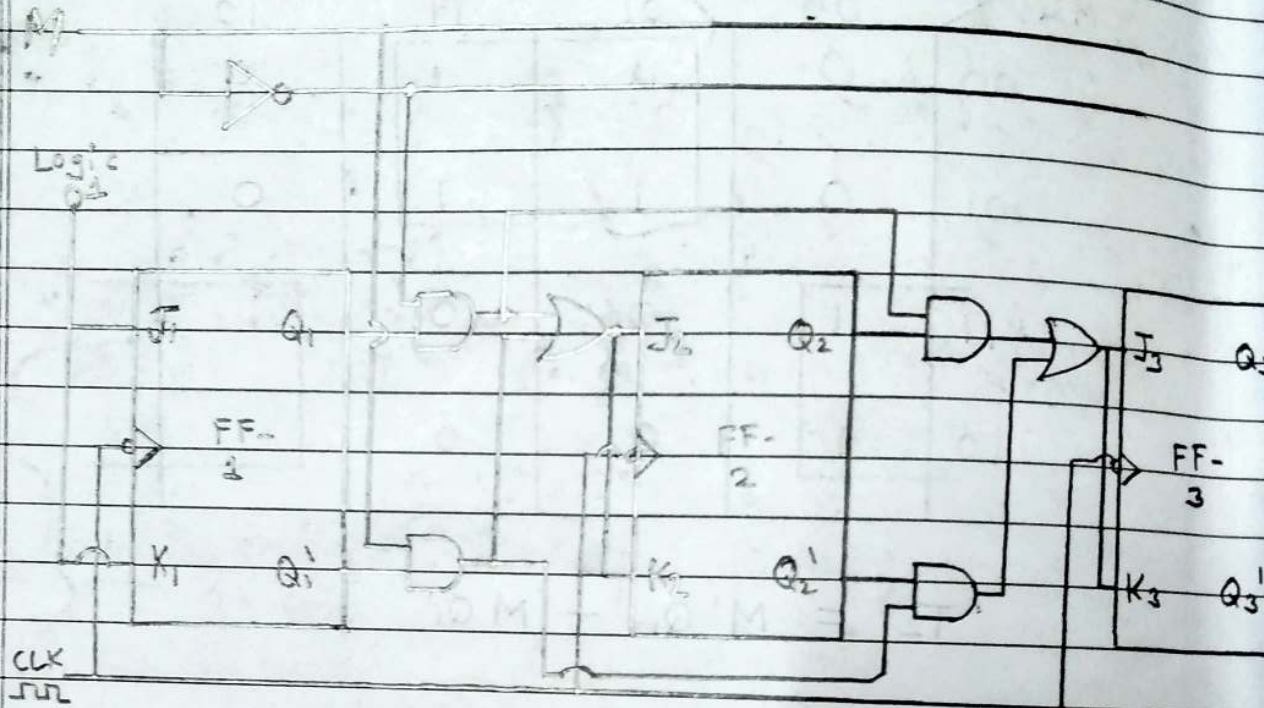
Designing of 3 bit synchronous UP-Down Counter.

Truth table :-

M	$Q_3$	$Q_2$	$Q_1$	$Q_3^*$	$Q_2^*$	$Q_1^*$	$T_3$	$T_2$	$T_1$
0	0	0	0	0	0	1	0	0	1
0	0	0	1	0	1	0	0	1	1
0	0	1	0	0	1	1	0	0	1
0	0	1	1	1	0	0	1	1	1
0	1	0	0	1	0	1	0	0	1
0	1	0	1	1	1	0	0	1	1
0	1	1	0	1	1	1	0	0	1
0	1	1	1	0	0	0	1	1	1

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- Circuit diagram :-



- Applications :-

The utility of synchronous counters span various applications, including :-

1. Machine Motor Control.
2. Motor RPM counter.
3. Rotary Shaft Encoders
4. Pulse Generators

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Title :- b. Modulus N counter

Problem Statement :- Realization of Mod-N counter using IC 7490.

Hardware and Software requirements :-

Theory :-

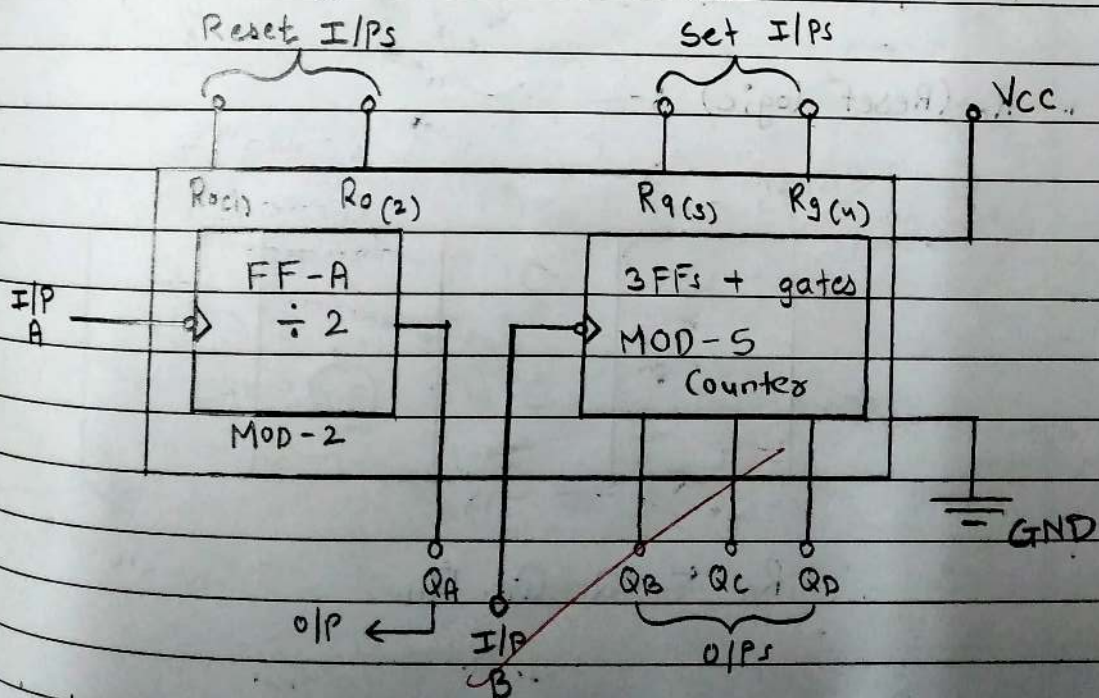
Modulus N Counter :

Modulus of a counter represents the number of states through which the counter progresses during the operation. It is denoted by N.

Thus MOD-N counter means the counter progresses through N states.

A Mod-4 counter will have 4 states.

IC 7490 Internal Structure :-



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- Design :-

Mod-7 :-

- Truth table :-

CLK	Q <sub>D</sub>	Q <sub>C</sub>	Q <sub>B</sub>	Q <sub>A</sub>	Reset
0	0	0	0	0	0
↓ (1)	0	0	0	1	0
↓ (2)	0	0	1	0	0
↓ (3)	0	0	1	1	0
↓ (4)	0	1	0	0	0
↓ (5)	0	1	0	1	0
↓ (6)	0	1	1	0	0
↓ (7)	0	1	1	1	1
↓ (8)	0	0	0	0	1

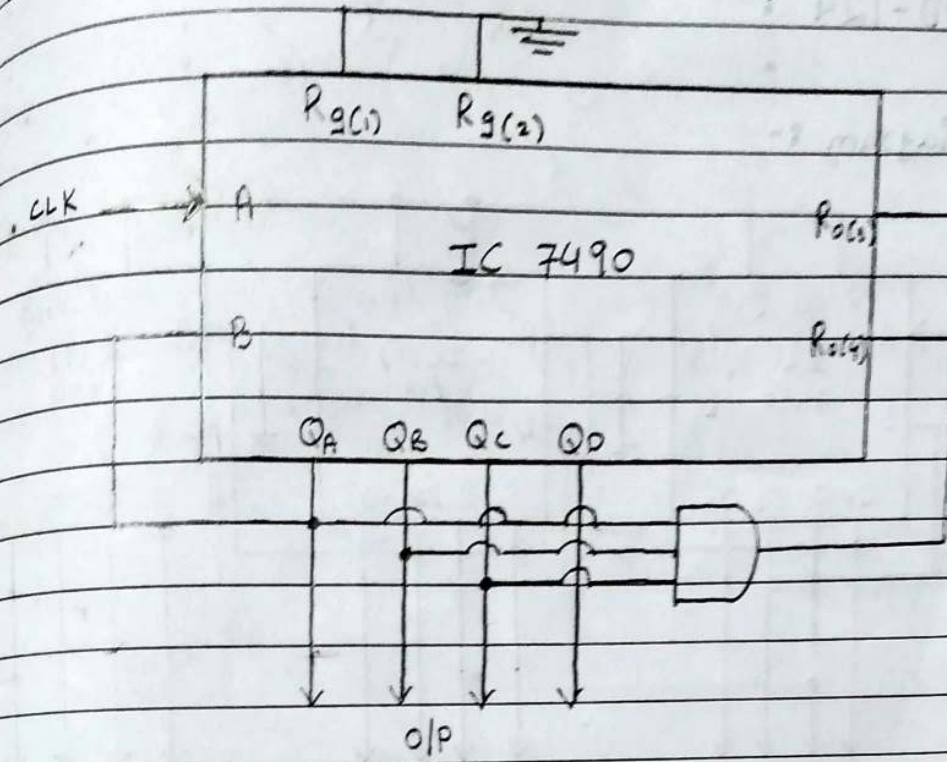
- K-Map :-

∴ R<sub>0</sub> (Reset logic) :-

		Q <sub>B</sub> Q <sub>A</sub>			
Q <sub>C</sub>		00	01	11	10
0		0	0	0	0
		0	1	3	2
1		0	0	1	0
		4	5	7	6

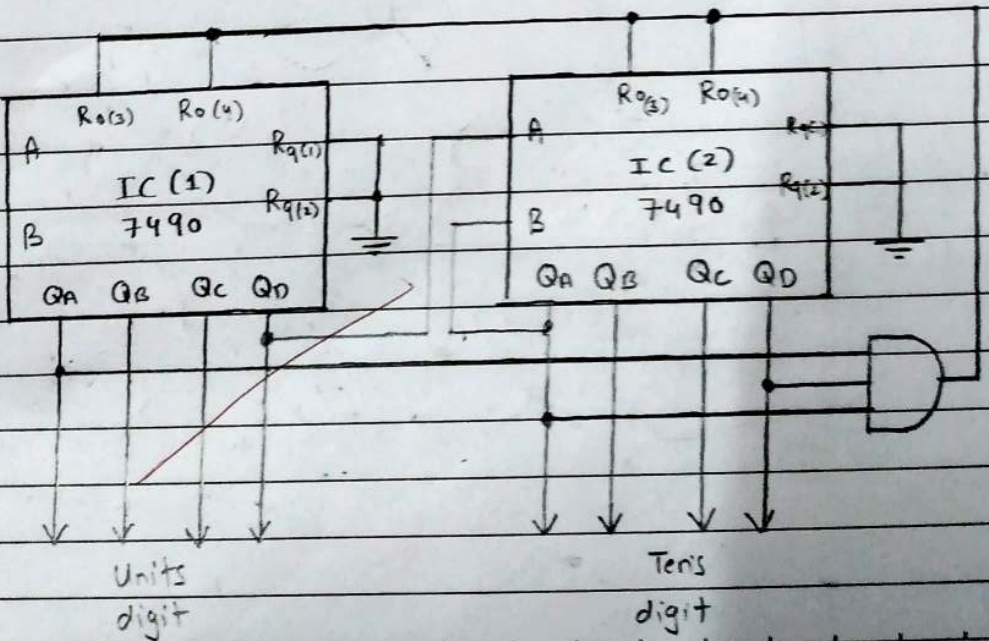
$$R_0 = Q_C \cdot Q_B \cdot Q_A$$

Diagram :-



Mod-98 :-

Diagram :-



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MOD-124 :-

- Diagram :-

