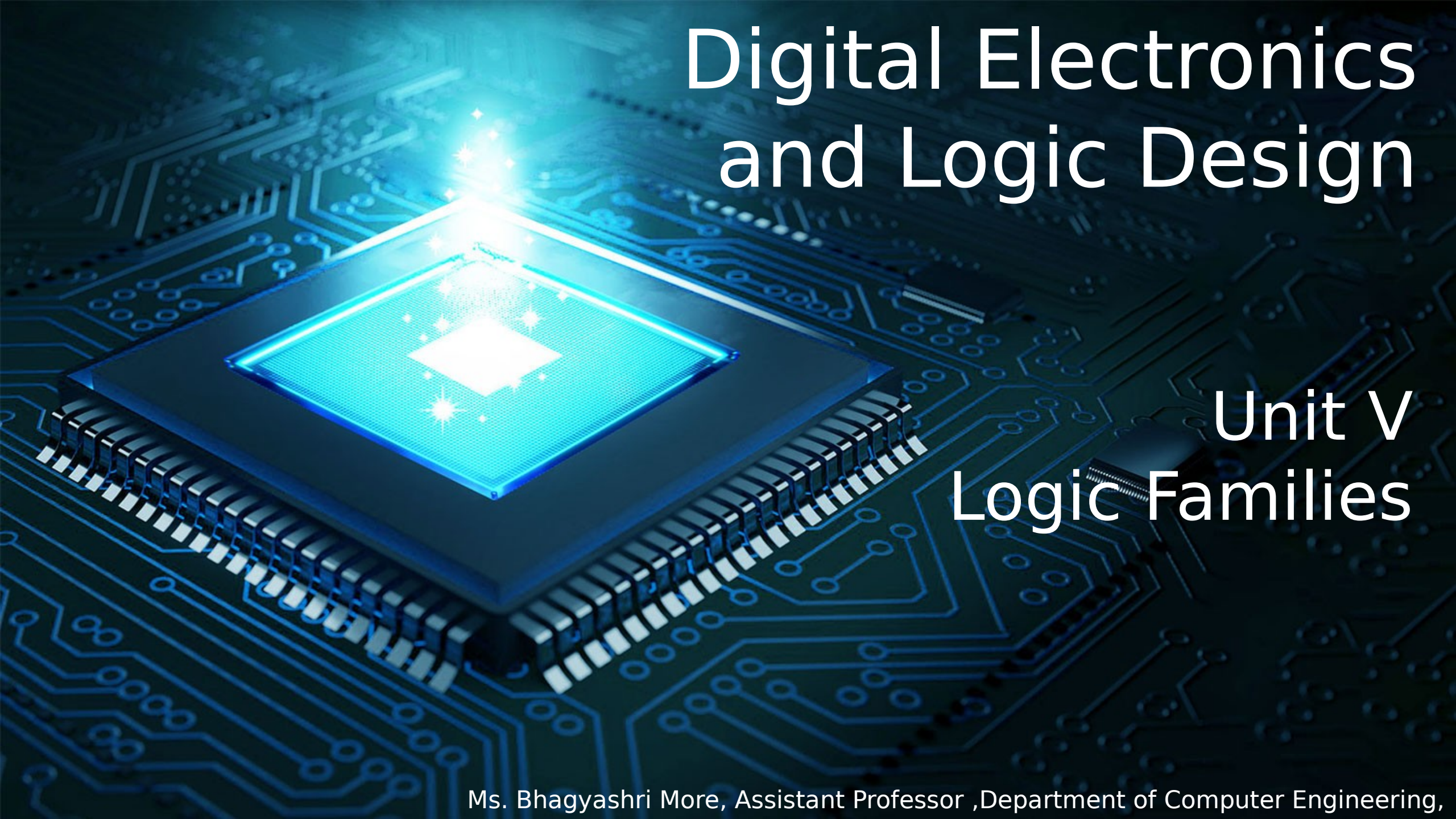


Digital Electronics and Logic Design

Unit V
Logic Families

Ms. Bhagyashri More, Assistant Professor ,Department of Computer Engineering,

Agenda

01

Classification of Logic Families: Unipolar and Bipolar Logic Families, Characteristics of Digital ICs: Fan-in, Fan-out, Current and voltage parameter, Noise immunity, propagation delay, Power Dissipation, Figure of Merits, Operating Temperature Range, Power supply requirements.

02

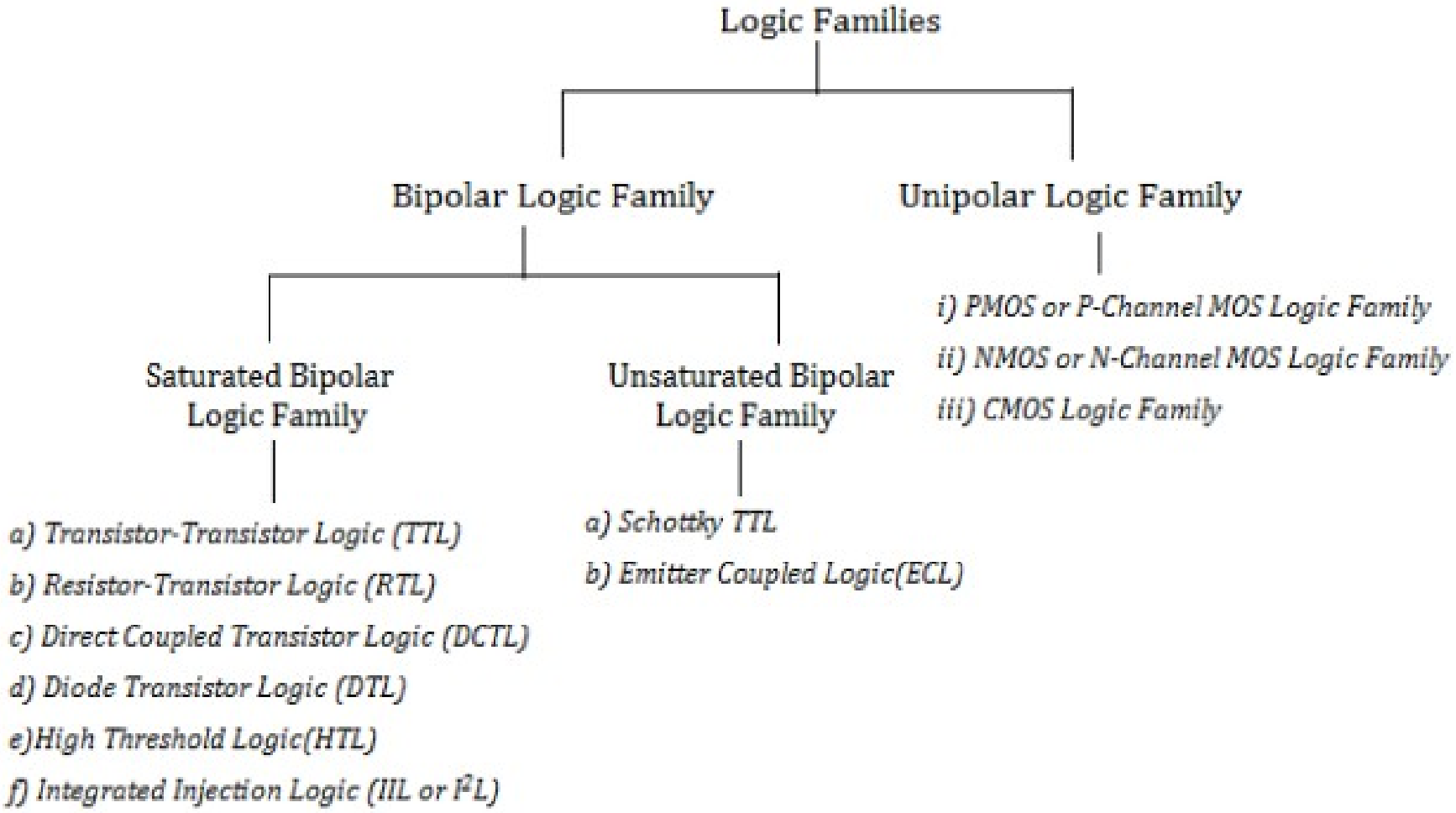
Transistors: Transistors Logic-Operation of TTL NAND gate (2 input NAND gate), TTL with active pull up, TTL with open collector output, wired AND gate connection, Tristate TTL devices, TTL characteristics, CMOS: CMOS inverter, CMS characteristics, CMOS configurations- wired logic, open drain outputs.

Digital Logic Families

- In Digital Designs, our primary aim is to create an Integrated Circuit (IC). A Circuit configuration or arrangement of the circuit elements in a special manner will result in a particular Logic Family.
- Low-cost electronics circuits whose components are fabricated on a single, continuous piece of semiconductor material to perform a high-level function. This IC is usually referred to as a monolithic IC first introduced in 1958. The digital ICs are categorized as,

1. Small scale integration SSI <12 no of gates
2. Medium scale integration MSI 12 to 99 no of gates.
3. Large scale integration LSI 100 to 9999 no of gates
4. Very large scale integration VLSI 10,000 or more

Classification of the Logic Families

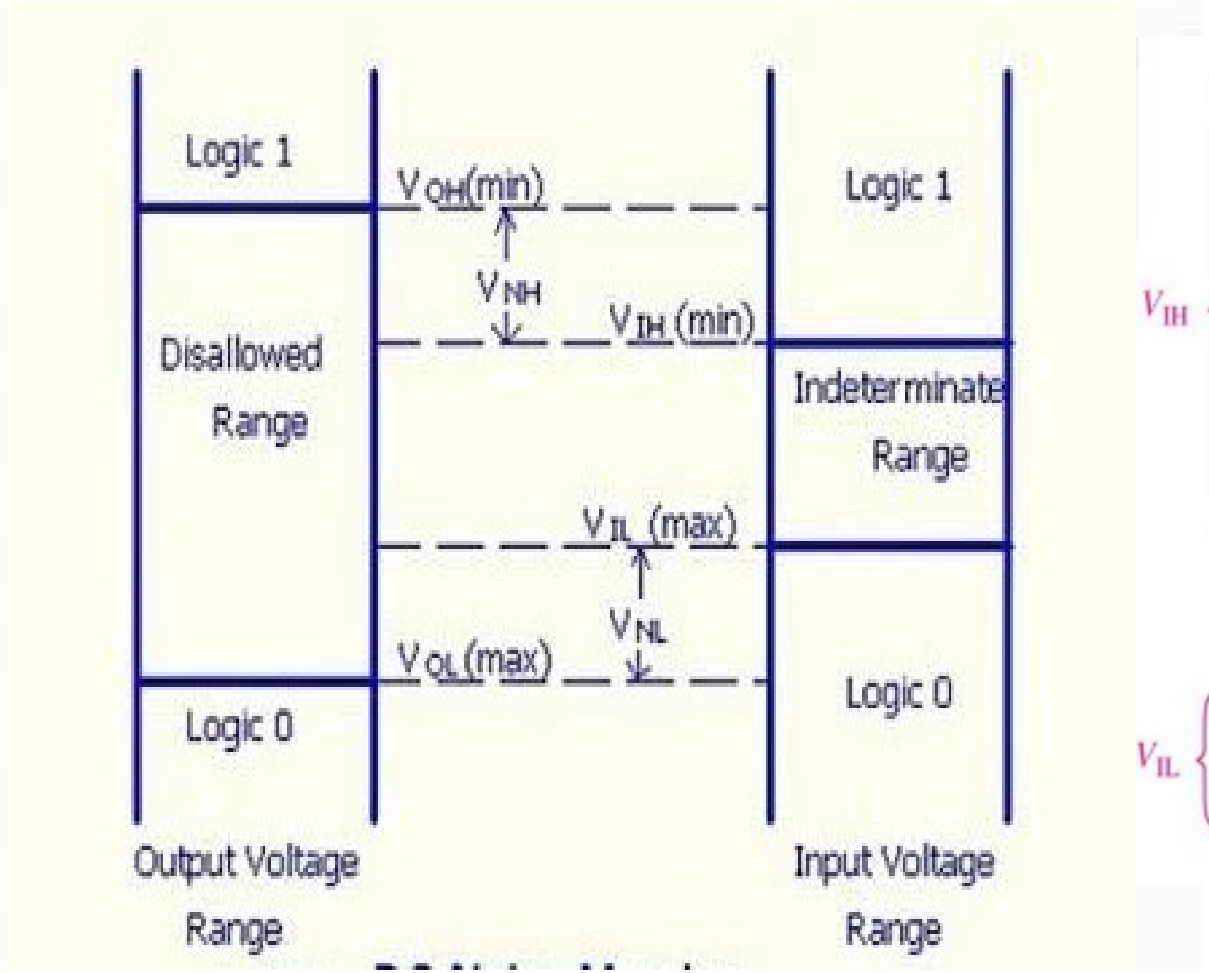


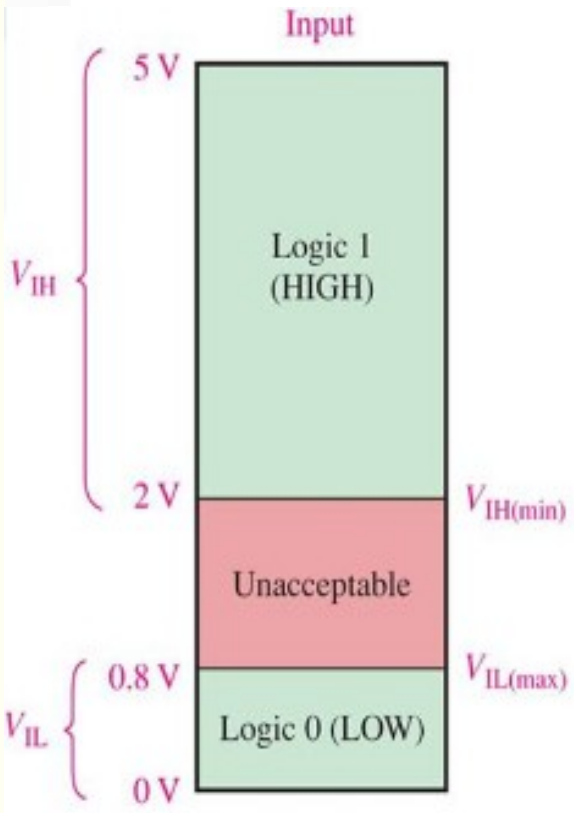
Characteristics of Digital ICs

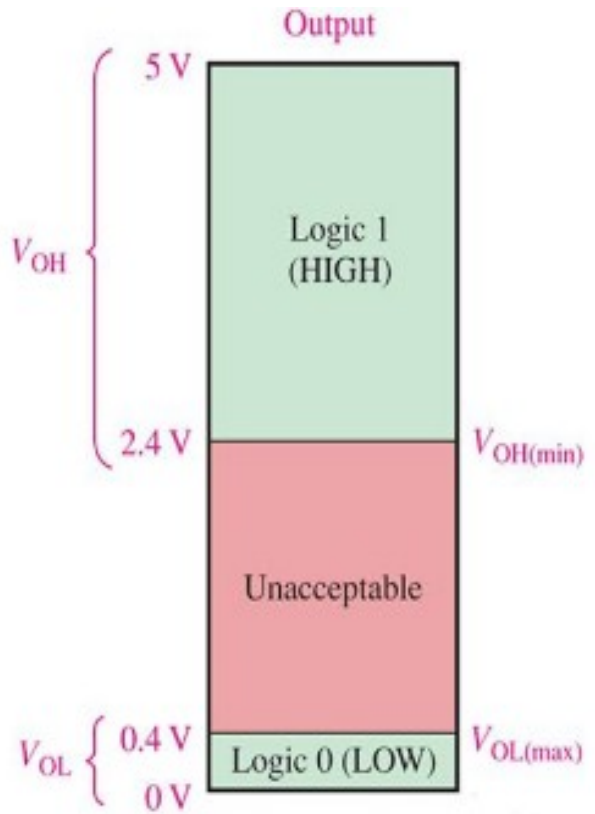
Input /Output voltage level:
The following currents and voltages are specified which are very useful in the design of digital systems.

1. **High-level input voltage, VIH** : This is the minimum input voltage which is recognized by the gate as logic 1.
2. **Low-level input voltage, VIL:** This is the maximum input voltage which is recognized by the gate as logic 0.
3. **High-level output voltage, VOH:** This is the minimum voltage available at the output corresponding to logic 1.
4. **Low-level output voltage, VOL:** This is the maximum voltage available at the output corresponding to logic 0.
5. **High-level input current, IIH :** This is the minimum current which must be supplied by a driving source corresponding to 1 level voltage.
6. **Low-level input current, IIL:** This is the minimum current which must be supplied by a driving source corresponding to 0 level voltage.
7. **High-level output current, IOH:** This is the maximum current which the gate can sink in 1 level.
8. **Low-level output current, IOL:** This is the maximum current which the gate can sink in 0 level.

Characteristics of Digital ICs



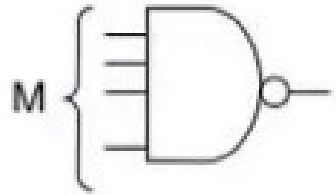




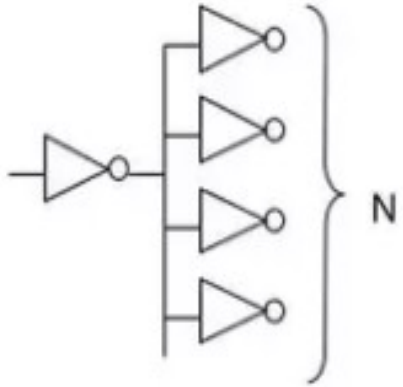
Voltage and current characteristics of TTL

Characteristics of Digital ICs

Fan-In: The fan-in of a logic gate is defined as the number of inputs (coming from similar circuits) that it can handle properly.



Fan-Out: In general, a logic circuit is required to drive several logic inputs. The fan-out (also sometimes called the loading factor) is defined as the maximum number of standard logic inputs that an output can drive reliably. For example, a logic gate that is specified to have a fan-out of 8 can drive 8 standard logic inputs. if this number exceeds the output logic-level voltages cannot be guaranteed.



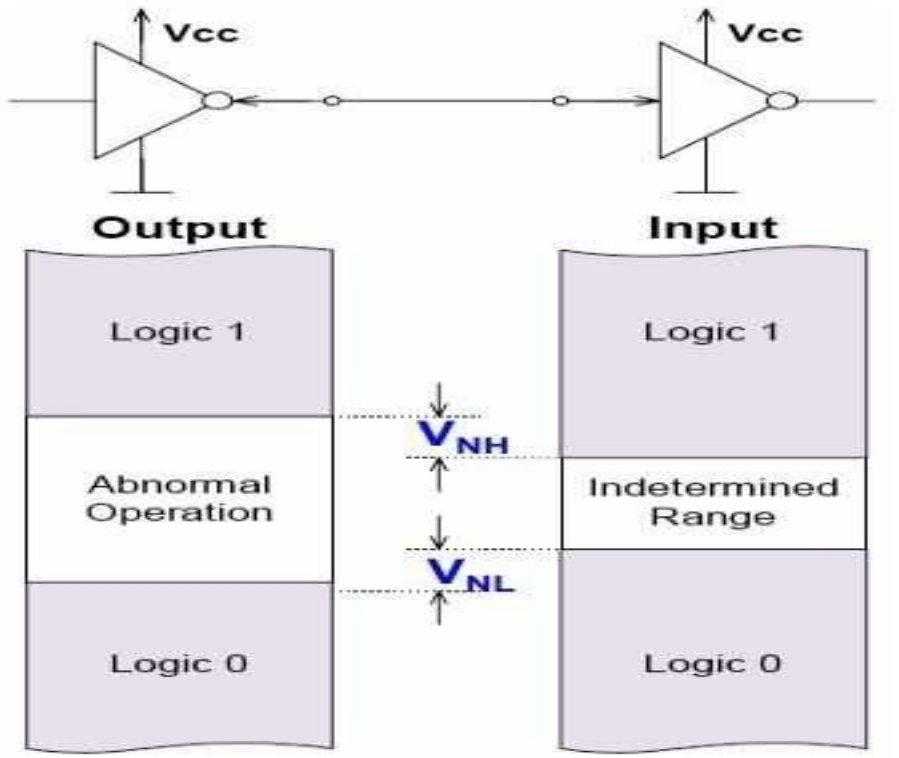
Characteristics of Digital ICs

Power Dissipation: This is the amount of power dissipated in an IC. It is determined by the current, Icc. that it draws from the Vcc supply and equals Vcc Icc where Icc is average value of Icc(0) and Icc(1). This power is specified in mW. Lower power dissipation is desirable feature for any IC.

The time required for the output of a digital circuit to change states after a change at one or more of its inputs. The speed of a digital circuit is specified in terms of the propagation delay time. The delay times are measured between the 50 percent voltage levels of input and output waveforms. There are two delay times, *tp*HL: when the output goes from the HIGH state to the LOW state and *tp*LH, corresponding to the output making a transition from the LOW state to the HIGH state. The propagation delay time of the logic gate is taken as the average of these two delay times.

Characteristics of Digital ICs

Noise Margin: Ability of the gate to tolerate fluctuations of the voltage levels. The input and output voltage levels defined above point. Stray electric and magnetic fields may induce unwanted voltages, known as noise, on the connecting wires between logic circuits. This may cause the voltage at the input to a logic circuit to drop below VIH or rise above VIL and may produce undesired operation. The circuit's ability to tolerate noise signals is referred to as the noise immunity, a quantitative measure of which is called noise margin.



$V_{NH} = V_{OH} - V_{IH}$

$V_{NL} = V_{IL} - V_{OL}$

Characteristics of Digital ICs

Propagation Delay: The time required for the output of a digital circuit to change states after a change at one or more of its inputs. The speed of a digital circuit is specified in terms of the propagation delay time. The delay times are measured between the 50 percent voltage levels of input and output waveforms. There are two delay times,

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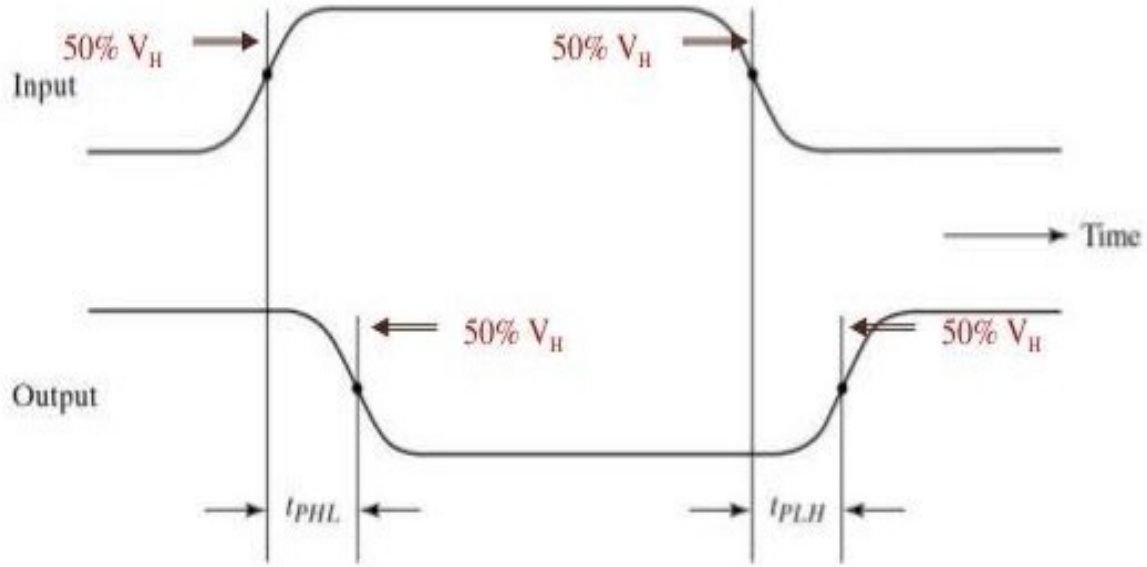


Characteristics of Digital ICs

Figure of merit:

The figure of merit of a digital IC is defined as the product of speed and power. The speed is specified in terms of propagation delay time expressed in nanoseconds.

Figure of merit = propagation delay time (ns) * power (mW)

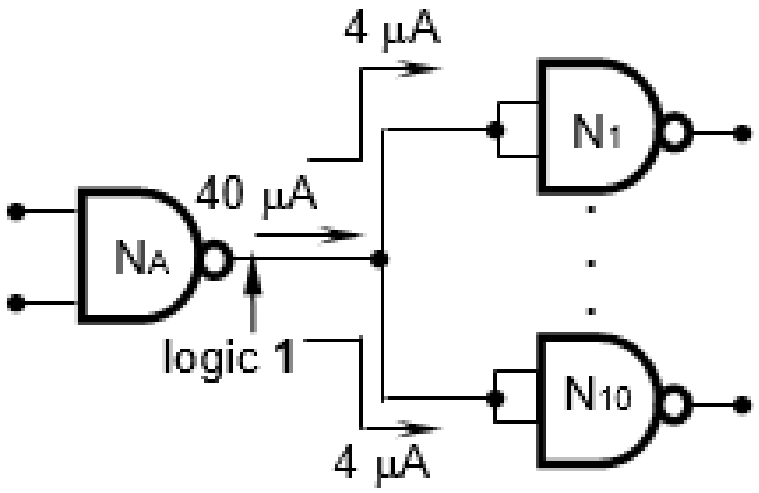
It is specified in **pico joules (ns * mW = pJ).**

A low value of speed-power product is desirable. In a digital circuit, if it is desired to have a high speed, low propagation delay time, then there is a corresponding increase in the power dissipation and vice versa.

Characteristics of Digital ICs

Current sourcing: When a load is connected to a device so that the device supplies current to the load (sources current) then the configuration is said to be current sourcing.

Current sinking: When a load is connected to a device so that current flows from the power supply through the load and into the device, then the configuration is said to be current sinking. When current flows into the device, it is said to be sinking current



g. 3.13 TTL current-sourcing operation

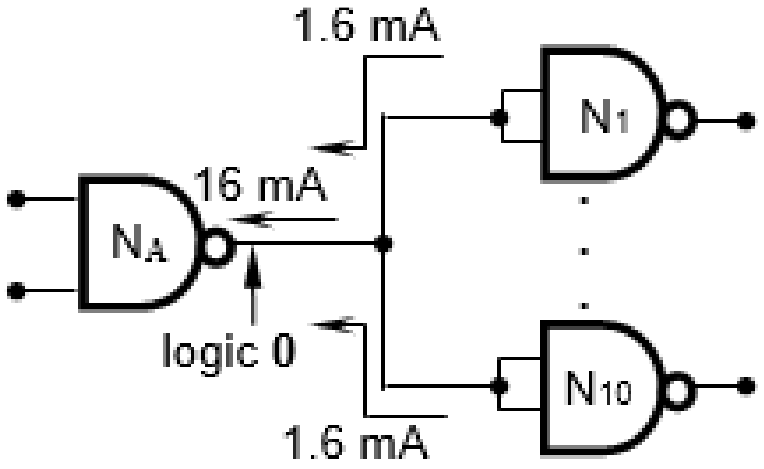
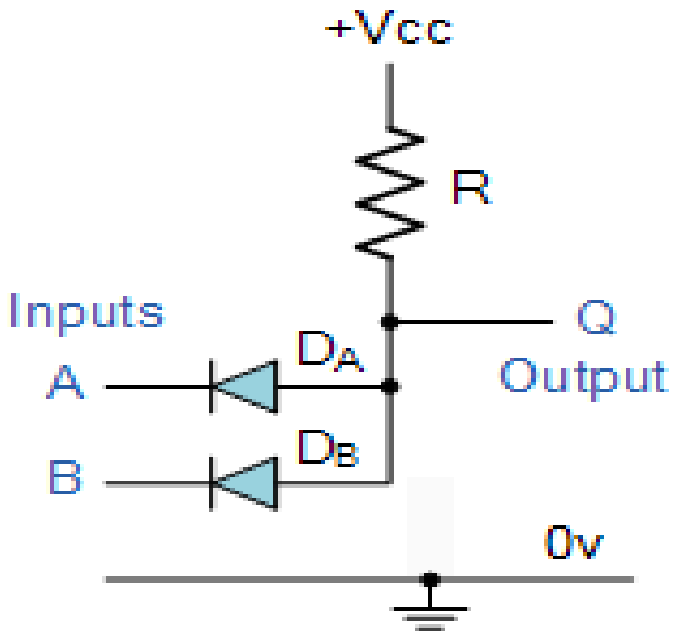


Fig. 3.14 TTL current-sinking operation

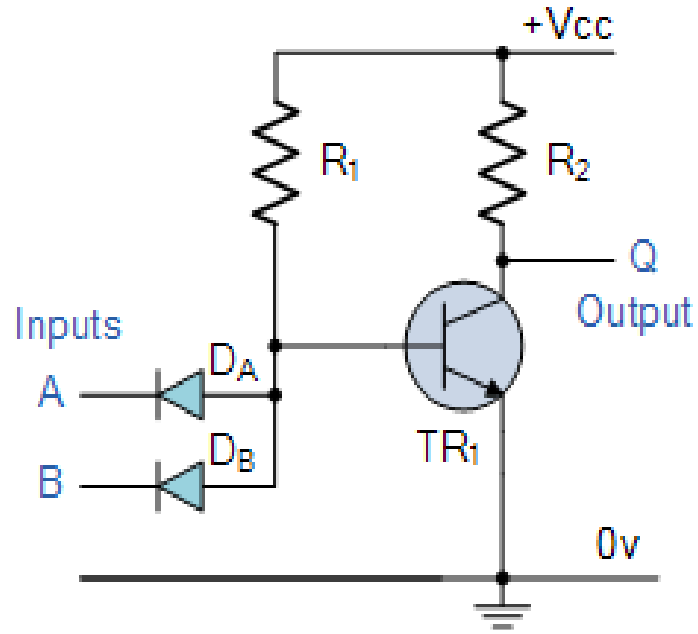
Simple Basic Digital Logic Gates

Simple digital logic gates can be made by combining transistors, diodes and resistors with a simple example of a Diode-Resistor Logic (DRL) AND gate and a Diode-Transistor Logic (DTL) NAND gate given below.

Diode-Resistor Circuit



Diode-Transistor circuit

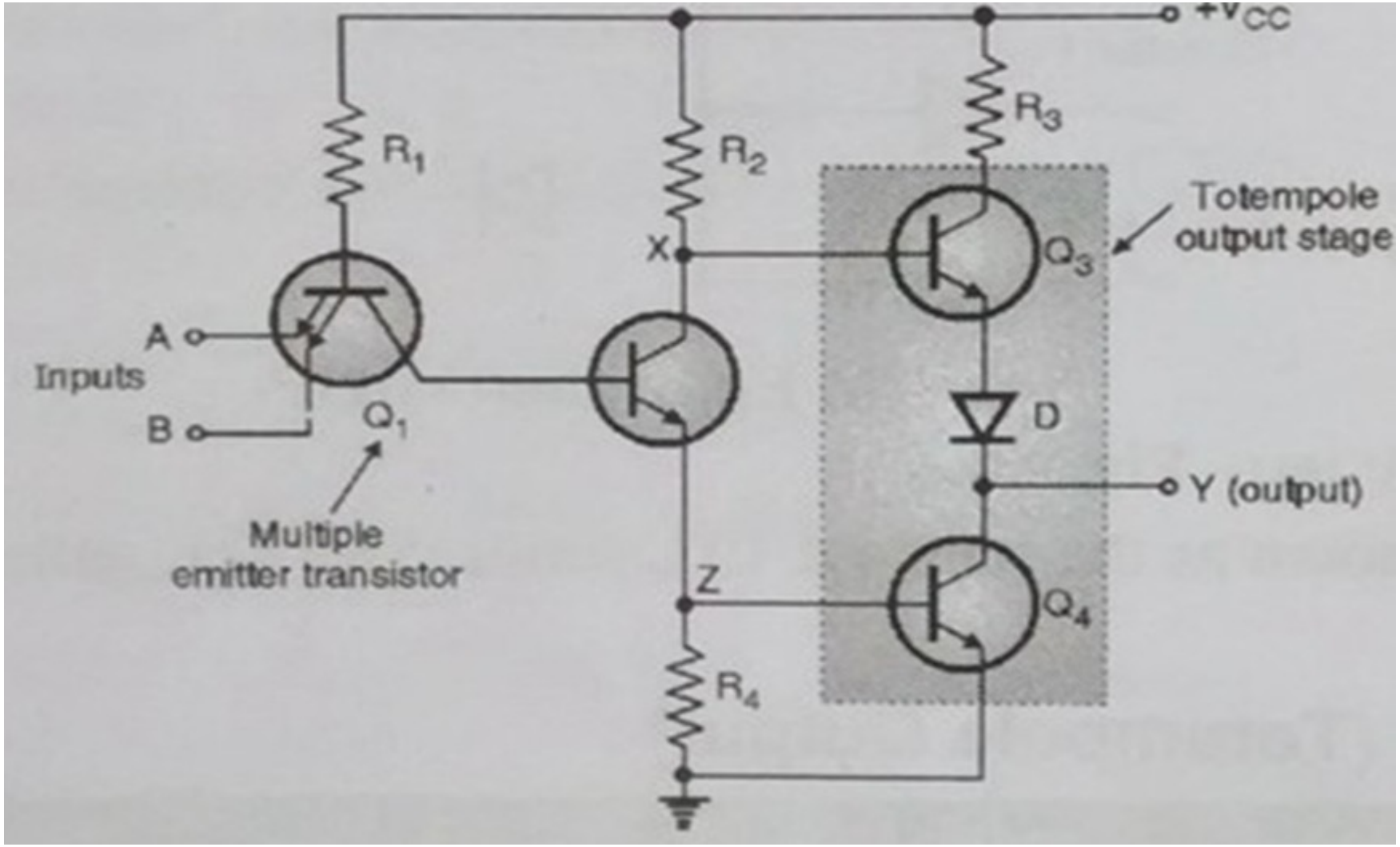


TTL Logic Gates

1. TTL stands for Transistor-transistor Logic. It is a logic family made up of, bipolar junction transistors (BJT s). Here, both the functions (logic and amplifying) are performed by the transistors; therefore, it is named as the Transistor-Transistor Logic. An ideal example of TTL logic IC would be Logic Gate ICs like the 7400 NAND or the 7402 NOR Gate.
2. TTL is the short form of transistor-transistor logic. TTL logic uses multiple transistors having multiple emitters and multiple inputs. The types of the transistor-transistor logic are Standard transistor-transistor logic, Fast transistor-transistor logic, Schottky transistor-transistor logic, High power transistor-transistor logic, Low power transistor-transistor logic, and Advanced Schottky transistor-transistor logic.
3. TTL logic gates are made up of the Bipolar junction transistors and resistors. There are many variants of TTL developed for various particular purposes like the radiation-hardened TTL packages for space applications and Low power Schottky diodes that can provide an excellent combination of speed and lesser power consumption.

Two Input TTL-NAND Gate (Totempole Output)

A	B	ON	OFF	A NAND B
0	0	Q1 Q3	Q2Q3	1
0	1	Q1 Q3	Q2Q3	1
1	0	Q1 Q3	Q2Q3	1
1	1	Q2Q4	Q1Q3	0



Two Input TTL-NAND Gate (Totempole Output)

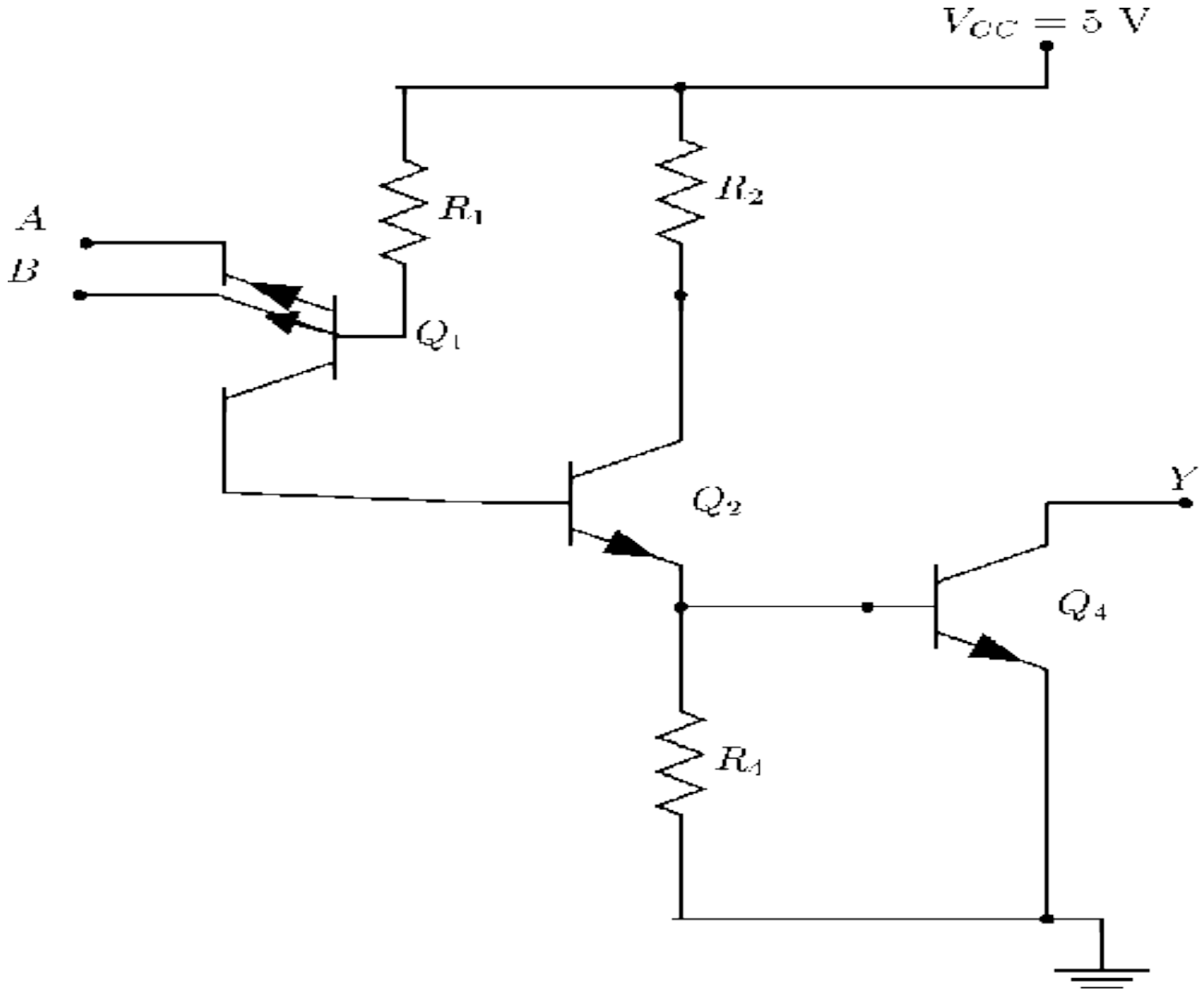
Operation:

a)A and B both low: both B-E junctions of Q1 are forward biased. Hence D1 and D2 will conduct to force the voltage at point C to 0.7V. This voltage is insufficient to forward bias B-E junction of Q2. Hence Q2 remains OFF. Therefore its collector voltage rises to VCC . As Q3 is operating in emitter follower mode, output Y will be pulled up to high voltage Y= 1

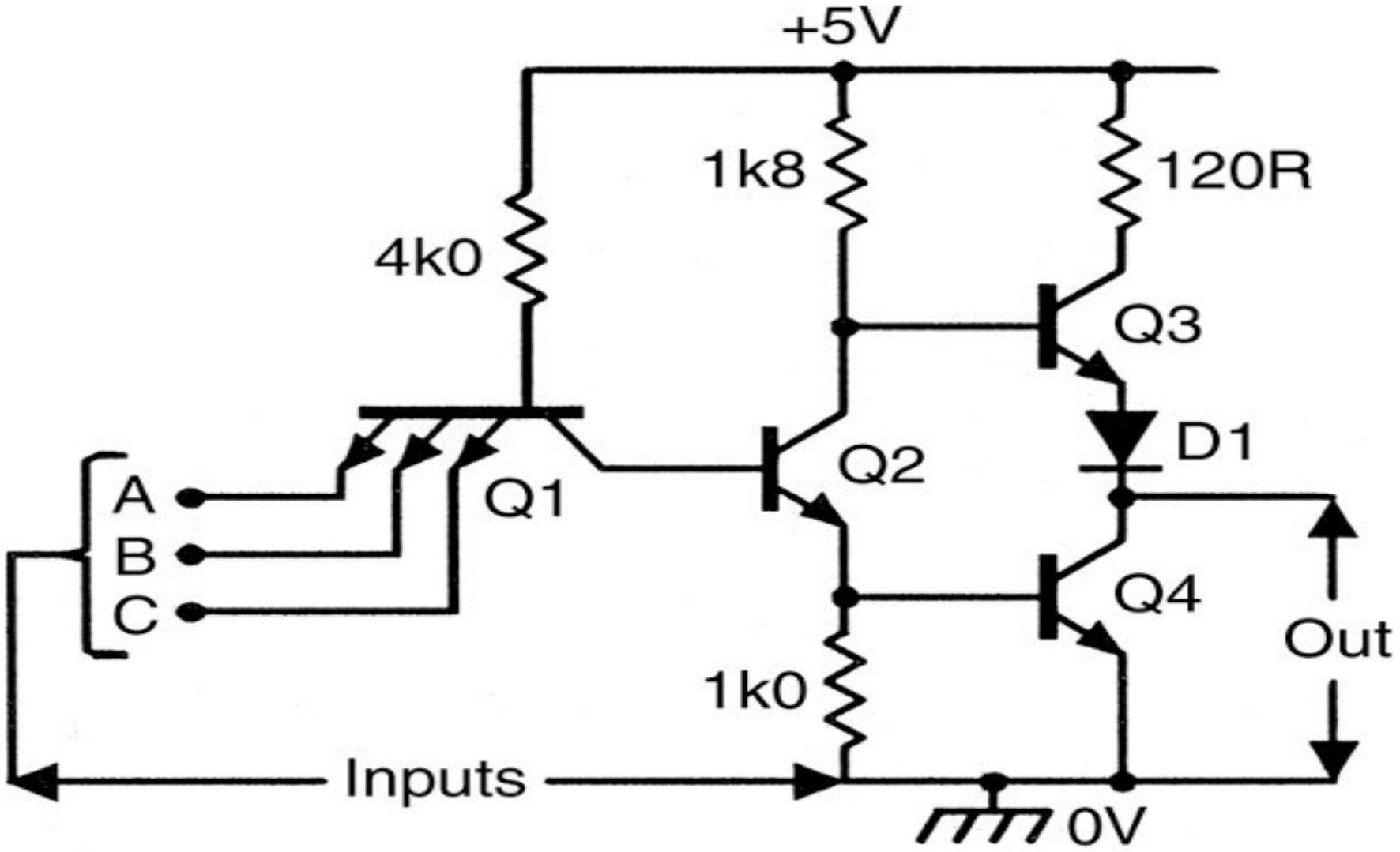
b)Either A or B low: If any one input is connected to ground with other left open or connected to VCC the corresponding diode (D1 or D2) will conduct. This will pull down voltage at C o 0.7V. This voltage is insufficient to turn on Q2 so it remains OFF. So collector voltage of Q2 will be equal to VCC. This voltage acts as base voltage for Q3. As Q3 acts as an emitter follower, output Y will be pulled to VCC. Y= 1

c)A and B both high: If both A and B are connected to then both diodes D1 and D2 will be reverse biased and do not conduct. Therefore D3 is forward biased and base current is supplied to transistor Q2 via R1 and D3. As Q2 conducts, the voltage at X will drop down and Q3 will be OFF, whereas voltage at Z will increase to turn ON Q4. As Q4 goes into saturation, the output voltage Y will be pulled down to low. Y = 0

Open Collector Output (TTL)



Three Input TTL NAND Gate



Advantages of TTL

1. TTL family is the fastest saturating logic family (working in between the saturation and cut-off modes). Also, TTL gates are available in a variety of forms, such as high-speed TTL, high-speed Schottky TTL, low-power TTL etc.
2. Typical supply voltage is only +5 V with a permitted variation of ±0.25 V. At present, TTL gates of 3-volt and even to 1.5-volt supply are possible.
3. It has good noise immunity. Typical noise-margin is about 0.4 V.
4. Power dissipation is in the range of several mW only. In the case of low-power Schottky TTL gates, this is less than 2 mW per gate.
5. TTL gates are compatible with other logic families.
6. Commercial and military versions of TTL gates are available.
7. These gates are more freely available in the open market than most other logic families.
8. Good fan-out; TTL gates can drive up to 10 gates.
9. TTL gates producing almost all of the logic functions are available in the market.
10. TTL gates exhibit low output impedance for high/low states

Disadvantages of TTL

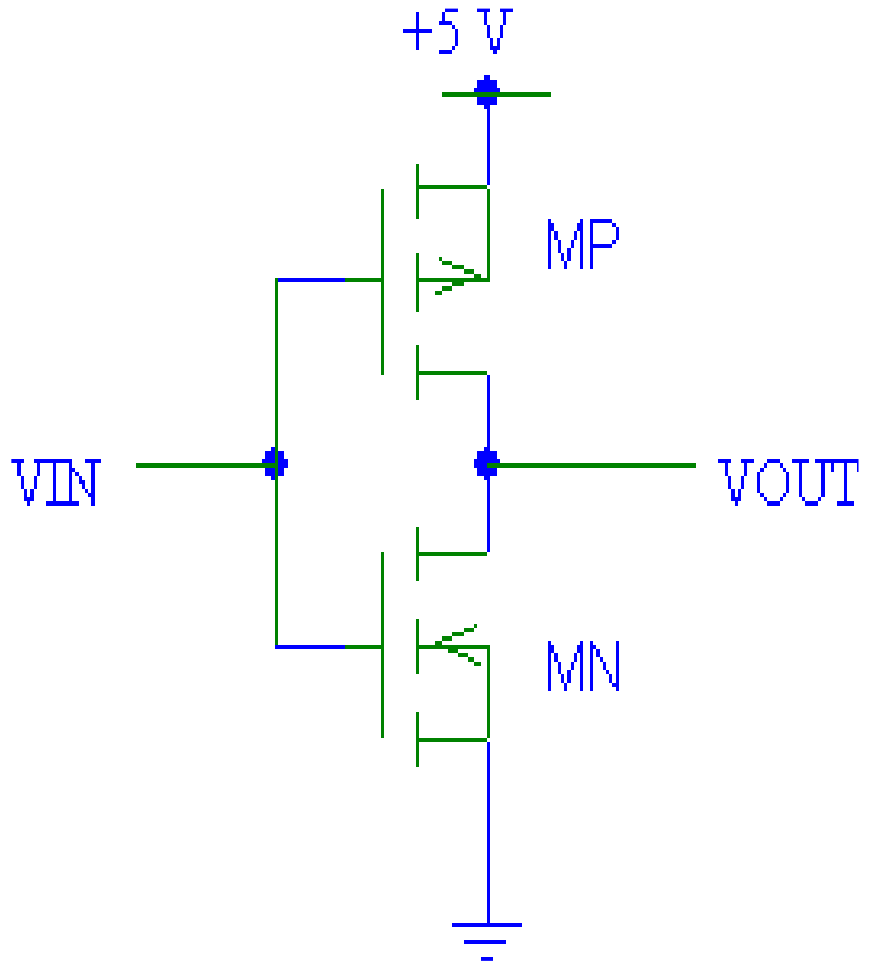
1. Noise immunity is not very high; so TTL gates cannot be used in applications where large noise voltages exist.
2. Because of isolation problems, which require more chip space, TTL VLSI circuits are not possible in its conventional form.
3. Power dissipation of TTL gates is much higher than that of MOS gates.
4. Cost of TTL gates is higher than that of NMOS/CMOS gates, when MSI and LSI gates are considered.
5. TTL gates generate transient voltages at switching instants.
6. Wired-OR capability is not possible for the conventional TTL gates; open-collector gates are required for this application.

CMOS Logic

1. The term CMOS stands for “Complementary Metal Oxide Semiconductor”. CMOS technology is one of the most popular technology in the computer chip design industry and broadly used today to form integrated circuits in numerous and varied applications. Today’s computer memories, CPUs and cell phones make use of this technology due to several key advantages. This technology makes use of both P channel and N channel semiconductor devices.
2. One of the most popular MOSFET technologies available today is the Complementary MOS or CMOS technology. This is the dominant semiconductor technology for microprocessors, microcontroller chips, memories like RAM, ROM, EEPROM and application specific integrated circuits (ASICs).

CMOS Inverter

1. A CMOS inverter contains a PMOS and a NMOS transistor connected at the drain and gate terminals, a supply voltage VDD at the PMOS source terminal, and a ground connected at the NMOS source terminal, were VIN is connected to the gate terminals and VOUT is connected to the drain terminals.
2. It is important to notice that the CMOS does not contain any resistors, which makes it more power efficient that a regular resistor-MOSFET inverter. As the voltage at the input of the CMOS device varies between 0 and 5 volts, the state of the NMOS and PMOS varies accordingly.



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