Total No. of Questions—**8**] [Total No. of Printed Pages—**4**

Seat No.	

[4657]-573

S.E. (Computer Engineering) (I Semester) EXAMINATION, 2014

DIGITAL ELECTRONICS AND LOGIC DESIGN

(2012 PATTERN)

Time : Two Hours **Maximum Marks : 50**

N.B. **:—** (*i*) Attempt Q. No. **1** *or* Q. No. **2**, Q. No. **3** *or* Q. No. **4**, Q. No. **5** *or* Q. No. **6** and Q. No. **7** *or* Q. No. **8**.

(*ii*) Figures to the right indicate full marks.

(*iii*) Assume suitable data, if necessary.

1. (*a*) Do the following conversions : [6]

(*i*) $(101110.0101)_2 \rightarrow (\quad)_{10}$

(*ii*) $(432A)_{16} \rightarrow (\quad)_2$

(*iii*) $(428.10)_{10} \rightarrow (\quad)_2$

P.T.O.

(*b*) Reduce the following using K-map techniques : [4]

$f(A, B, C, D) = \Pi(0, 2, 3, 8, 9, 12, 13, 15)$.

(*c*) What is logic family ? Give the classification of logic family. [2]

Or

2. (*a*) Minimize the following expression using Quine-McClusky : [6]

$f(A, B, C, D) = \Sigma m\ (0, 2, 3, 6, 7, 8, 10, 12, 13)$.

(*b*) Explain with neat diagram two input CMOS NAND gate. [6]

3. (*a*) Explain Look Ahead Carry generator in detail. [6]

(*b*) Explain with neat diagram working of serial- n serial-out 4-bit shift register. Draw necessary timing diagram. [6]

Or

4. (*a*) Explain rules for BCD addition with suitable example and design one digit BCD adder using IC 7483. [6]

(*b*) Design given sequence generator using J-K FF. Sequence is $1 \rightarrow 3 \rightarrow 5 \rightarrow 6 \rightarrow 7 \rightarrow 1$ [6]

5. (*a*) Draw the ASM chart for the following state machine. A 2-bit up counter is to be designed with output $Q_A Q_B$, and enable signal 'X'. If X = 0, then counter changes the state as 00 —01 — 10— 11 — 00. If 'X' = 1, then counter should remain in current state. Design the circuit using JK-FF and suitable MUX. [7]

(*b*) Write VHDL code for 4-bit adder using structural modeling style. [6]

Or

6. (*a*) Write a VHDL code for 8 : 1 MUX using Behavioural modeling. [7]

(*b*) Draw an ASM chart, state diagram and state table for synchronous circuit having the following description.

The circuit has control input C, clock and outputs *x*, *y*, and *z*.

(*i*) If C = 1, on every clock rising edge the code on output *x*, *y* and *z* changes from 000 — 010 —100 — 110 — 000 and repeats.

(*ii*) If C = 0, the circuit holds the present state. [6]

7. (*a*) Draw and explain Basic architecture of FPGA in detail. [6]

(*b*) Implement the following functions using PLA : [7]

$f_1(A, B, C) = \Sigma m(0, 3, 4, 7)$

$f_2(A, B, C) = \Sigma m(1, 2, 5, 7)$.

Or

8. (*a*) A combinational circuit is defined by the functions :

$f_1(A, B, C) = \Sigma m(3, 5, 7)$

$f_2(A, B, C) = \Sigma m(4, 5, 7)$.

Implement the circuit with PLA having 3 input and 3 product term with 2 output. [7]

(*b*) Implement 4 : 1 MUX using PAL. [6]