Total No. of Questions—8] [Total No. of Printed Pages—4

Seat No.	

[4757]-1073

S.E. (Computer Engg.) (First Semester) EXAMINATION, 2015

DIGITAL ELECTRONICS AND LOGIC DESIGN

(2012 PATTERN)

Time : Two Hours **Maximum Marks : 50**

N.B. :— (*i*) Answer Q. No. **1** *or* Q. No. **2**, Q. No. **3** *or* Q. No. **4** and Q. No. **5** *or* Q. No. **6** and Q. No. **7** *or* Q. No. 8.

(*ii*) Figures to the right indicate full marks.

(*iii*) Assume suitable data, if necessary.

1. (*a*) Minimize the following function using K-map and realize using logic gates : [4]

$$F(A, B, C, D) = \sum m\ (1, 5, 7, 13, 15) + d(0, 6, 12, 14)$$

(*b*) Convert the following : [2]

$$(46)_{10} = (?)_8$$

(*c*) List the differences between CMOS and TTL. [6]

P.T.O.

Or

2. (*a*) Convert the following numbers into binary numbers ? [4]

(*i*) $(37)_8$

(*ii*) $(25.5)_{10}$

(*b*) Explain standard TTL characteristics in detail. [6]

(*c*) Represent the following signed number in 2's complement method : [2]

(*i*) +25

(*ii*) –25

3. (*a*) Design a 3-bit excess 3 to 3-bit BCD code converter using logic gate. [6]

(*b*) Design mod-5 synchronous counter using J-K flip-flop. [4]

(*c*) Draw the excitation table of J-K flip-flop. [2]

Or

4. (*a*) Design a 4-bit binary to Gray code converter circuit using logic gates. [4]

(*b*) Design a Mod 20 counter using decade counter IC7490. [6]

(*c*) Perform the following : [2]

$(11011)_2 + (0101)_2 = (?)_2$

5. (*a*) State and explain basic component of ASM chart ? Also explain the salient features of ASM chart. [7]

(*b*) Write VHDL code 4 : 1 multiplexer using behavioural and data flow modelling style. [6]

Or

6. (*a*) Design a sequence generator circuit to generate the sequence 1–2–3–7–1 using Multiplexer controller based ASM approach. Consideration : [7]

(*i*) If control input C = 0, the sequence generator circuit in the same state.

(*ii*) If control input C = 1, the sequence generator circuit goes into next state.

(*b*) Explain the following statements used in VHDL with suitable examples : [6]

(*i*) CASE

(*ii*) With select-when

(*iii*) Loop statement.

7. (*a*) Comparison between PROM, PLA and PAL. [7]

(*b*) Draw and explain the basic architecture of FPGA. [6]

Or

8. (*a*) A combinational circuits is defined by the function : 7

$F_1(A, B, C) = \sum m\ (0, 1, 3, 7)$

$F_2(A, B, C) = \sum m\ (1, 2, 5, 6)$

Implement this circuit with PLA.

(*b*) A combinational circuits is defined by the function : 6

$F_1\ (A, B, C) = \sum m\ (0, 1, 5, 6, 7)$

Implement this circuit with PAL.