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Assignment-I (Microprocessor)

Q1. Explain addressing modes of 80386 with examples

Ans.
- Addressing modes indicate a way of locating data or operands.
- The 80386 Microprocessor provides 11 addressing modes:-

1) Register addressing mode:-
- The data is stored in a register and it is referred using a particular register.
- All register accept IP used in this addressing mode.
- eg: ADD EAX, EBX

2) Immediate addressing mode:-
- In this addressing mode, immediate data is part of instruction.
- The 8/16/32 bit data required to execute an instruction is given directly along with the instruction is called "Immediate addressing mode".
- eg: mov EAX, 12345678 H

3) Direct addressing mode:-
- The 8/16/32 bit data required to execute an instruction is present in memory location and effective address of this memory location is is given directly along with the instruction then it is called "Direct addressing mode".
- eg: mov AX, [5000H]

4) Register indirect addressing mode:-
- A base register will contain the address of operand.
- Eg: mov [ECX], EDX.

5) Based addressing mode:-
- A BASE register's contents is added to a DISPLACEMENT to form the operands offset.

- Eg: mov ECX, [EAX+24]

6) Index addressing mode:-

- An INDEX register's contents is added to a DISPLACEMENT to form the operands offset.
- eg: ADD EAX, TABLE [ESI]

7) Scaled index addressing mode

- An INDEX ~~x~~ register's contents is multiplied by a scaling factor which is added to a DISPLACEMENT to form the operands offset.
- eg: mov EBX, LIST [ESI *4]

8) Based Index addressing mode

- The contents of a BASE register are added to the contents of an INDEX register to form the effective address of an operand.
- eg: mov EAX, [ESI][EBX]

9) Based Scaled Index addressing mode

- The contents of an INDEX register is multiplied by a SCALING factor and the result is added to the contents of a BASE register to obtain the operands offset.
- eg: mov ECX, [EDX*8], [EAX]

10) Based Index addressing mode with Displacement

- The contents of an INDEX register and a BASE registers contents and a DISPLACEMENT are all summed together to form the operand effect.
- eg: ADD EDX, [ESI][EBP+ 00FFFFF OH]

11) Based Scaled Index addressing mode with Displacement

- The contents of an INDEX register are multiplied by a SCALING factor, the result is added to the contents of a BASE register and a DISPLACEMENT to form the operand's offset.
- eg: mov EAX, LIST [EDI*4][EBP +80]

Q2. Draw and explain architecture of 80386 DX.

Ans. The internal architecture of 80386DX is divided into 3 sections:

i) Central Processing Unit (CPU)

i) Execution unit

- The execution unit reads the instruction from the instruction queue and executes the instructions.
- It consists of three subunits:

→ Control unit:

- It contains microcode and special hardware.
- The microcode and special hardware allows 80386 DX to reduce time required for execution of multiply and divide instructions.

→ Data unit:

- The data unit contains the ALU, eight 32-bit general purpose registers and a 64-bit barrel shifter.
- The barrel shifter is used for multiple bits shifts in one clock.

→ Protection test unit:

- The protection test unit checks for segmentation violations under the control of the microcode.

ii) Instruction Decode Unit:

- The instruction decode unit takes instruction bytes from the code prefetch queue and translates them into microcode.

2) memory management unit (MMU):

i) ~~iii)~~ Segmentation unit:

- The segmentation unit translates logical addresses into linear addresses at the request of the execution unit.
- The segmentation unit compares the effective

address for the length limit specified in the segment descriptor.

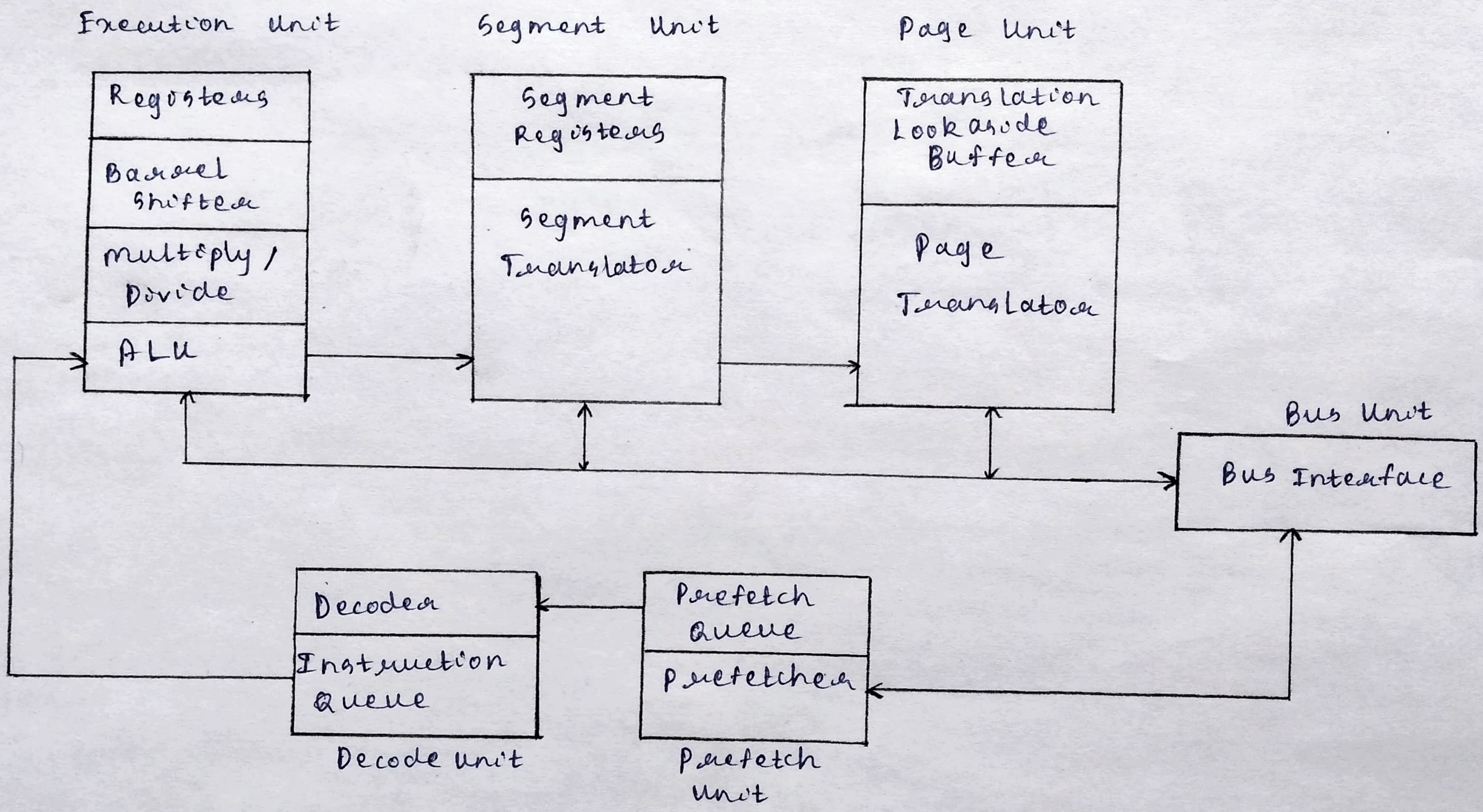
ii) Paging unit:

- When the 80386 DX paging mechanism is enabled, the paging unit translates linear addresses generated by the segmentation unit or the code ~~fo~~ prefetch unit into physical addresses.
- If paging unit is not enabled, the physical address is the same as the linear address, and no translation ~~unit~~ is necessary.

3) Bus control unit:

- The Bus Control unit is the 80386 DX's communication with the outside world.
- It provides a full 32-bit bi-directional data bus and 32-bit address bus.
- The ~~bus~~ bus control unit is responsible for the following operations:

1. It accepts internal requests for code fetch and for data transfers from the code fetch unit and from execution unit.
2. It sends address, data and control signals to communicate with memory and I/O devices.
3. It controls the interface to external bus masters and coprocessors.


Execution Unit
Registers
Barrel Shifter
multiply / Divide
ALU
Segment Unit
Segment Registers
Segment Translator
Page Unit
Translation Look aside Buffer
Page Translator
Bus Unit
Bus Interface
Decoder
Instruction Queue
Decode Unit
Prefetch Queue
Prefetcher
Prefetch Unit