## SPPU-SE-COMP-CONTENT - KSKA Git

Total No. of Questions : 4]			nestions : 4] SEAT No. :	SEAT No. :	
PA-4978			[Total No. of Page	es: 2	
			[6008]-230		
S.E. (Computer) (Insem.)					
MICROPROCESSOR					
(2019 Pattern) (210254) (Semester - II)					
		Hour]		: 30	
			the candidates: wer Q1 or Q2, Q3 or Q4.		
	1) 2)		wer Q1 or Q2, Q3 or Q4. week to the right indicate full marks.		
	<i>2)</i>	rigu	dies to the right that care full marks.		
<b>Q</b> 1)	a)	Exp	plain the architecture of the 80386 microprocessor with an appropr	riate	
<b>L</b> -/	,	_	gram.	[5]	
	,				
	b)	Des	scribe the following addressing modes of 80386 with example	[6]	
		i)	Index addressing mode		
		1)	mack addressing mode		
		ii)	Direct addressing mode		
		•••	D 11 1 C S S S S S S S S S S S S S S S S		
		iii)	Based index mode	20	
	c)	Desc	scribe the use of various 80386 Data Movement Instructions in assen	nbly	
	,		guage programming with examples.	<u>[</u> [4]	
				9	
			OR .S		
<b>Q</b> 2)	a)	Desc	scribe the various operating modes of 80386.	[5]	
	b)	Desc	scribe the following addressing modes of 80386 with example	[6]	
		i)	Register addressing mode		
		ii)	Register Indirect addressing mode		
		_/			
		iii)	Immediate addressing mode		
	<u>a)</u>	Eva	Nain the Canaral Degisters and Seament Degisters of 90296 with	h on	
	c)	_	plain the General Registers and Segment Registers of 80386 with ropriate diagram.	14]	

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**Q3**) a) Explain the 80386 processor state after Reset. **[5]** Draw and Explain Read Cycle with non-pipelined address timing. b) [5] Draw and Explain Control Registers of 80386. **[5]** c) Explain the following signals [5] **Q4**) a) i) ii) iii) HOLD iv) NMI v) Draw and explain the Write Cycle with non-pipelined address timing.[5] b) Draw and Explain Debug Registers of 80386. [5]

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